model 8300

DIGITAL VOLTMETER

FLUKE®

STUDENT HANDOUT

Introduction

This training course has been prepared by the Customer Service Department of the John Fluke Mfg. Co., Inc. to assist the experienced technician to understand how the instrument works, how to calibrate it and how to maintain it. This manual is intended as a supplement to the Audio/Visual training package of the same title. It is suggested that prior to attending this course of instruction, the course titled "Recirculating Remainder" should have been completed. Should you have any questions, comments or suggestions about this course of instruction please feel free to communicate them to the Training Department by letter or telephone.

Customer Service Training Dept.

John Fluke Mfg. Co., Inc.

P.O Box 7428 • Seattle, Washington 98133

Tel: (206) 774-2409

Litho in U.S.A. 1-73

I. BLOCK FUNCTIONS: (Figure 1)

A. Power Supply

The Power supply furnishes five voltages used in the instrument. +18, −18 operating supplies, +190 volt readout tube supply, +5 volt logic supply and +7 volt reference supply. Provisions are made for auxiliary supply of 5 volts required in the Data Output Unit option.

B. Buffer

The Buffer board assembly includes Function switching components. It has an input impedance that is greater than 10^{12} with an insertion current less than 50 pa. The Input Attenuator offers three ratios of voltage division 1/1, 1/10 and 1/100. Input limiting is provided to prevent damage to the instrument in any range with up to 1100 volts applied.

The total gain of the Buffer is 1 inverted with a low impedance output. Input filtering is included in this assembly which consists of a 60 Hz notch filter and a 3 pole low pass (30 Hz) filter. All frequencies above 50 Hz are attenuated by more than 60 db.

C. A-D Converter

Inverting Amplifier is used only when the input voltage being measured is negative. When the input to the instrument is positive, FET switches cause the output of the Buffer to bypass the Inverting Amplifier.

Polarity Detector circuitry automatically detects the polarity of the input signal and provides outputs for the logic switching of the Inverting Amplifier.

A-D Amplifier has two fixed gains and is one of the key elements in the Recirculating Remainder system of analog digital conversion system.

Ladders and Switches provide a voltage back to the summing junction of the A-D Amplifier and also a discrete voltage that is stored in the Analog Storage for use when the instrument is in the Storage Mode of operation.

Sample and Hold circuitry provides storage for the remainder voltages while the instrument is in the Measurement Mode of operation.

Analog Comparitor provides current to the Current Controlled Oscillator whenever the output of the A-D Amplifier exceeds the reference voltage of 7 volts.

D. Logic Section

A clock which operates at a frequency of 666 Hz produces a pulse train of 1.5 ms pulses, providing the timing for the entire instrument.

A 6 State Register divides the Clock pulses into six discrete time periods, which correspond to the ZERO time and the five digit times used in the instrument

Current Controlled Oscillator provides a pulse train whose output pulses are proportional in repetition rate to the current being supplied it. The pulses supplied by this oscillator are fed to the 16 State Binary Counter for decoding.

16 State Binary Counter receives the pulses from the Current Controlled Oscillator and converts them to Binary Coded Decimal (BCD) output in the standard 1-2-4-4 output.

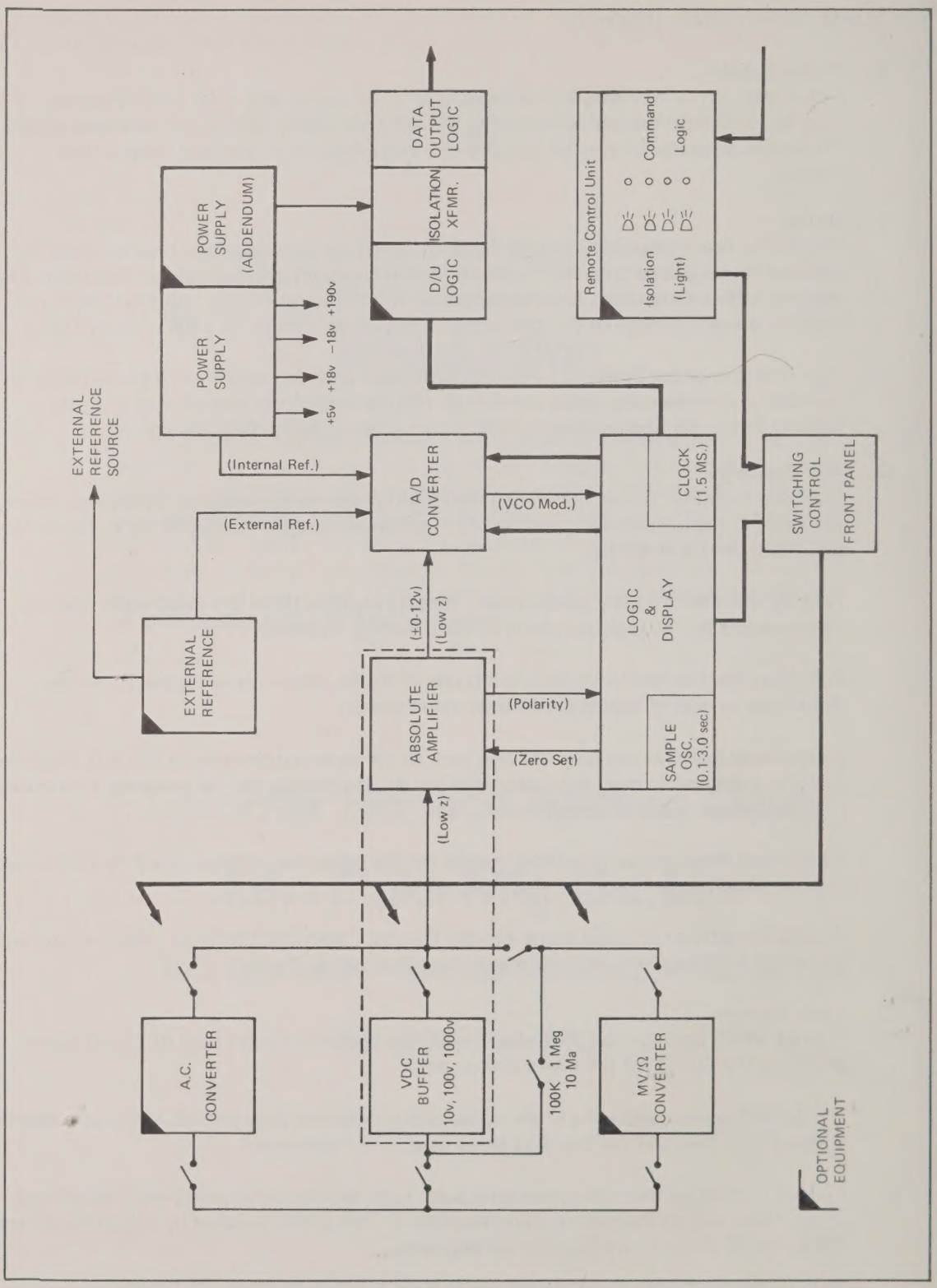


FIGURE 1. BASIC BLOCK DIAGRAM

Manual Range Controls are interlocked mechanically and electrically so as to provide priority to manual selections of function and range, preventing erroneous dial function or range commands.

Auto Range Controls are provided to accomplish automatic selection of the proper range via reed relays and functional logic packs.

Sample Oscillator provides a variable sample rate from once every 3 seconds to once every 100 milliseconds. Provisions for external sample rates up to 25 milliseconds are included.

Logic Section provides the solid state switching commands for both range and function controls.

E. Display

Anode Strobing circuit pulses each readout tube on for 1.5 ms during the appropriate time period of each complete cycle of the instrument. This means that during every 18 millisecond recycle period of the instrument each readout tube is only on for 1.5 milliseconds.

The BCD output of the 16 State Binary Counter is fed to the Decoder Driver where it is translated into decimal output. If the BCD code was 5 the Decoder Driver will apply ground to the five line to all readout tubes. Q31 through Q35 are enabled by the time period pulses A, B, C, D, E and the F pulse applied to the common emitters thus allowing the +190V to be applied to the proper readout tube for displaying the digits in sequence.

F. AC Converter

The input impedance is 1 megohm into the inverting amplifier. The gain is controlled by feedback switching. Rectification is accomplished by dual section half wave diodes.

Filtering is accomplished by a 3 section RC filter combined with large feedback loop capacitors. The output of the filter is fed to a times 10 Inverting Amplifier which feeds the A-D Converter of the instrument.

G. Millivolt/Ohms Converter

In millivolt operation a chopper stabilizer operational amplifier is used which feeds an intergrated circuit operational amplifier with a gain of 10 on the 1000 millivolt scale and a gain of 100 on the 100 millivolt scale. The output of the millivolt section of the converter is 0 to 12 volts DC.

In Ohms operation the converter uses the +7 volt reference to supply current to the unknown resistance and the voltage drop across the resistor is translated by the instrument into ohms values. The instrument input is so configured as to provide modified four terminal resistance measurements for additional accuracy.

H. External Reference

This option provides a means of referencing the instrument to external sources from 2 to 10.5 volts via a chopper stabilized operational amplifier to increase the isolation between the system under measurement and the 8300.

II. SUB-SECTION FUNCTIONS

A. **Power Supplies (Figure 2 and Schematic No. 5)**

The primary windings are so configured as to provide either 115 VAC or 230 VAC input power which is selected by a switch on the rear panel.

The +18 volt supply is zener regulated and provides the initial reference for the other supplies, so if trouble exists in the +18 supply it is reasonable to expect that all of the other supplies will also show a problem.

The −18 volt supply is referenced to the +18 volt supply by the voltage drop across R231, R223.

The +5 volt supply, which is used for the logic functions is regulated by the voltage drop appearing across the +18 volt supply and R229.

The +7 volt reference supply is regulated by zener pack A201. The voltage to this circuit is fed by the +18 volt supply.

The +190 volt supply for the readout tubes is regulated by a voltage division which is referenced to the +18 volt supply.

B. **Buffer (Figures 3, 4, 5, 6 and Schematic No. 1)**

The buffer pre-amplifier of the 8300A is basically an inverting unity gain voltage follower. Its primary function is to provide an impedance conversion between the signal source being measured and the A-D Converter input.

Referring to Figure 3, the buffer could be represented as shown. The input resistance of the buffer is $\frac{E_s}{I_s}$. If I_s can be kept small, then the impedance will be high. The resistance R_L is the leakage resistance between the High and Low input termianls. Care was taken in the mechanical design of the instrument so that the leakage resistance would always be greater than 10^{12} ohms.

The other component of I_s is I_e. Elementary feedback theory indicates that the input resistance of an amplifier connected as shown in Figure 3 will be the product of the open loop input resistance and the loop gain. Junction Field Effect J-FETs, are used in the inputs of the buffer, and thus an open loop input resistance of greater than 10^9 ohms is obtained. The loop gain of the buffer is approximately 10^6, so the input resistance of the actual amplifier is greater than 10^{15} ohms, or much greater than the leakage resistance than could be expected at the input terminals.

Using J-FETs also helps keep the insertion current of the buffer preamplifier less than 50 pa. That means that a source resistance of 1 megohm would cause less than 50 μV or ½ digit of offset due to injection current.

The A-D converter has a full scale input of 12 volts, thus requiring a means of reducing input signals greater than 12 volts, if they are to be measured. For that purpose, a 10 megohm attenuator can be placed in front of the buffer when the input exceeds 12V.

The attenuator has two ratios available. One provides a division of 10 and the other provides a ratio of 100. Both are controlled by the front panel switches or the Remote Control Unit. In the 1000 volt range, the divider ratio is 1/100 and in the 100 volt range the ratio is 1/10. In the 10 volt range the input is direct.

The attenuator connection is as shown in Figure 4, with range commands adjacent to each switch. Limiting circuits are provided at the amplifier input, in series with current limiting resistors so that ±1100 volt signals cannot damage the buffer, even in the 10 volt range.

A zeroing circuit (R47) is provided on the buffer for calibration. The excellent zero stability of the FET pair used at the buffer input makes it unnecessary to provide front panel adjustment.

In addition to providing impedance buffering and signal attenuation, the buffer pre-amplifier also can be called upon to filter the input signal. Internal to the amplifier are roll off networks

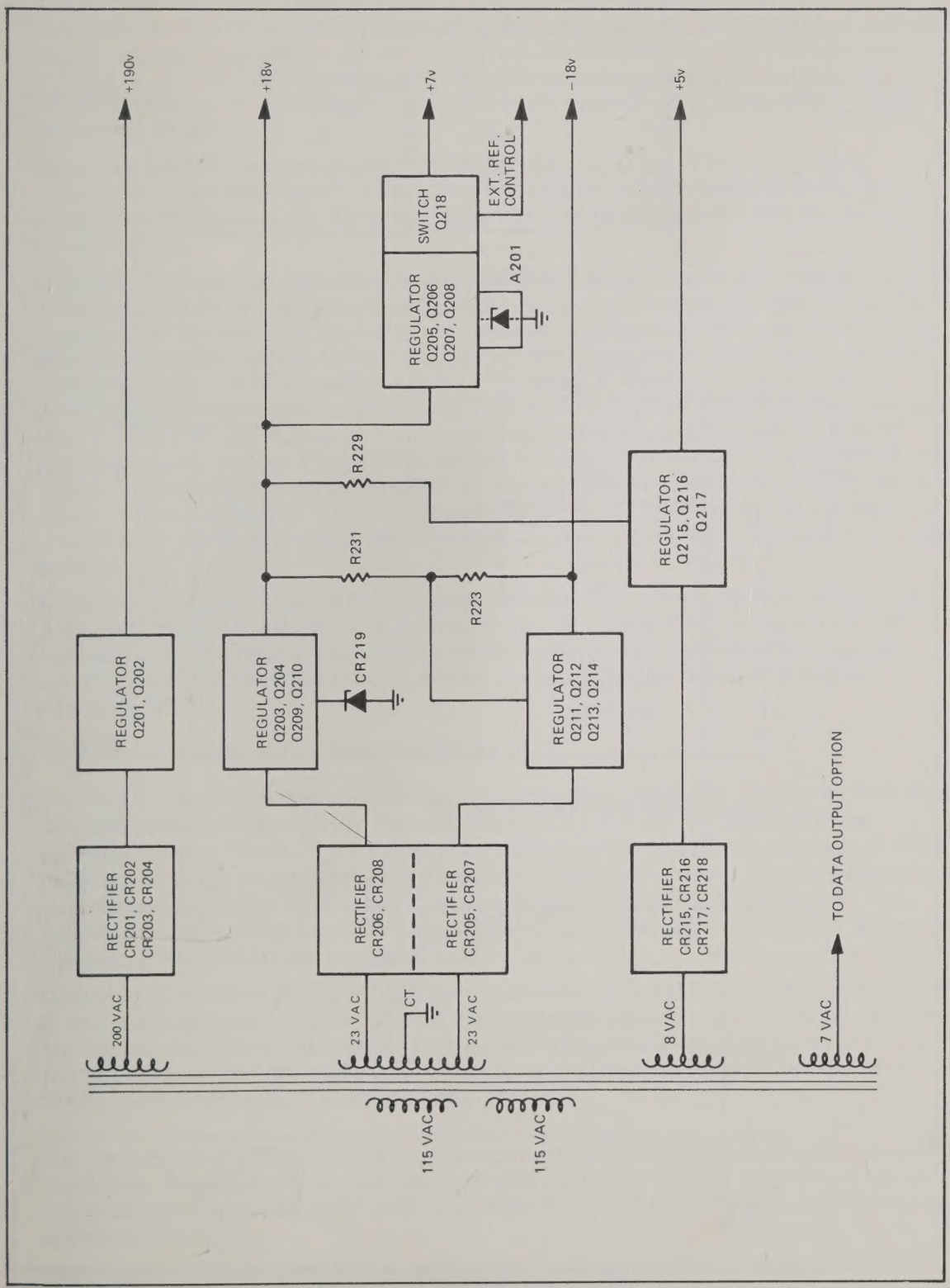


FIGURE 2. 8300A POWER SUPPLY

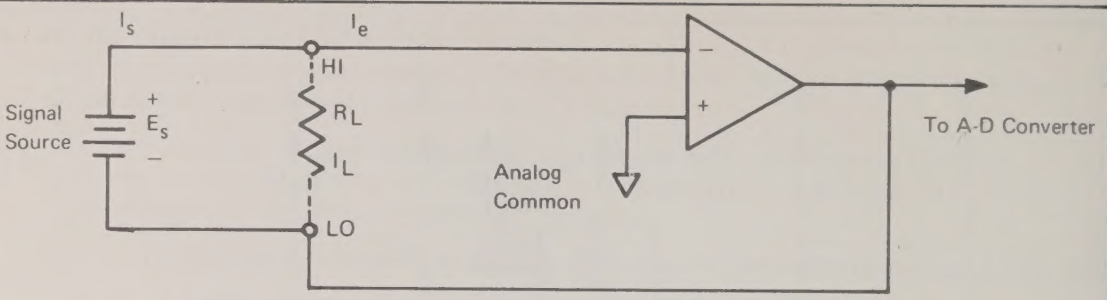


Figure 3. BUFFER

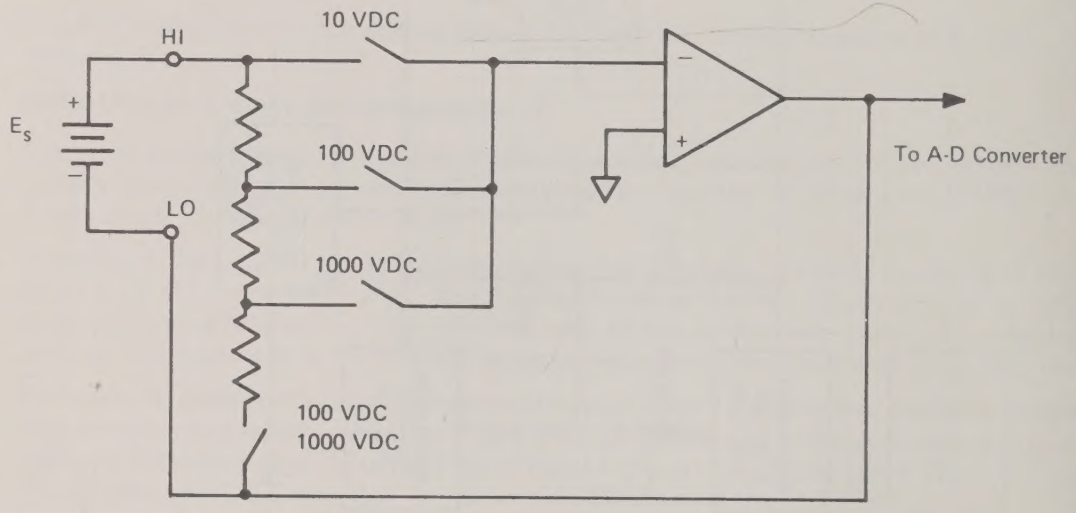


Figure 4. BUFFER WITH ATTENUATOR

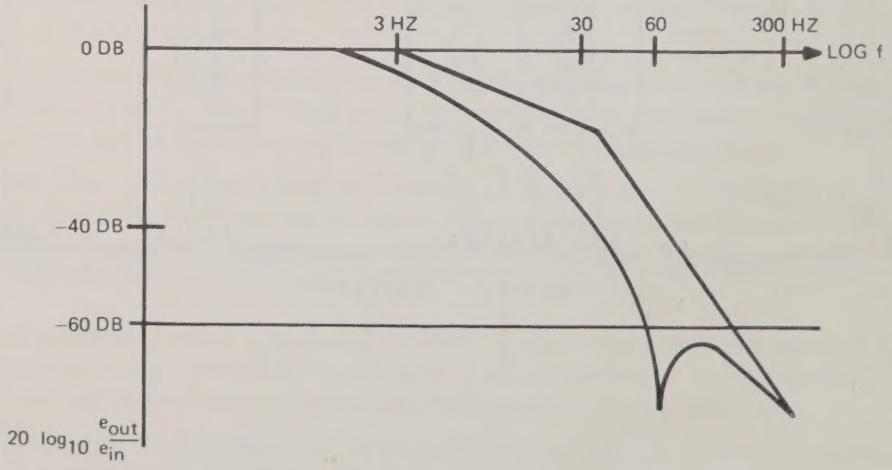


Figure 5. FILTER TRANSFER FUNCTION

that establish a unity gain frequency of 3 Hz. This roll off of the gain of the buffer provides high frequency filtering by attenuating the AC signals inside the buffer and presenting a reduced version of the AC signal input to the A-D Converter. The frequency characteristics are shown in Figure 5. A notch filter is provided at 60 Hz and three pole response is present above 30 Hz. As the figure shows, for all frequencies above 50 Hz, the rejection of AC signal at the input is greater than 60 db.

Up to now the buffer has been considered as a single block amplifier. A more detailed explanation of circuit operation is in order. The block diagram shown in Figure 6 is complete enough for signal tracing. For illustration, place a positive DC voltage across the HI and LO input terminals.

Since AMP 1 is a high gain operational amplifier with its inverting terminal grounded, any signal at the non-inverting terminal will produce a large in -phase version of that signal at the amplifiers output. AMP 2 is connected inside of its own feedback loop to give a negative gain of about 2.5. When the amplified positive signal at the output of AMP 1 is applied to AMP 2's loop, the result is that the output of AMP 2 is driven negative. The voltage to which the output of AMP 2 is driven is determined solely by the input signal applied and the voltage to which the non-inverting input of AMP 1 is driven. Since the loop gain of the buffer is very high, the positive input of AMP 1 effectively does not change, and as pointed out earlier, the FET input does not allow any current flow from the source. Because there is no voltage present with respect to the analog common at the positive input of AMP 1, and because no current can flow from the source, the output of AMP 2 can only go to $-E_S$ with respect to analog common. Thus, we have an inverting voltage follower.

When FILTER is called with the 8300, large capacitors are placed in the feedback paths of both AMP 1 and AMP 2. In addition, both a notch filter and a low pass filter are placed in the forward gain path. The feedback capacitors force the 3 Hz unity gain bandwidth for the buffer, the notch filter provides 60 Hz filtering, and the low pass filter adds two additional poles at effectively 30 Hz.

C. A/D Converter (Figures 7, 8, and Schematic No. 2)

Referring to Figure 7 the time relationships can more easily be visualized. The Master clock generates timing pulses, which are fed to the clock input of a J-K flip-flop, 3F, which produces the F and $\overline{F}$ pulses. The F pulse is further modified by Q1 where the $\overline{H}$ pulse is generated. The $\overline{H}$ pulses are fed to the clock inputs of the 6 State Shift Register, where five of the six timing pulses are generated. The sixth, $\overline{ZERO}$ pulse is generated by the action of the NAND gate 4B. Note that it is possible to divide any of the time periods into two equal parts by using the F and/or the $\overline{F}$ pulses. (These time periods are refered to as A1, A2, B1, B2 . . . etc.)

During the ZERO time period the $\overline{ZERO}$ pulse operates the A-D Auto Zero Drive Circuit. Q118 conducts and connects the output of A2 to the zero holding capacitor C115 and at the same time the input of the amplifier is grounded. This operation places the offset of A2 across C115 and effectively removes it for the remainder of the cycle. A similar circuit removes the offset from the Inverting Amplifier during "C" period of time.

For the purposes of illustration, it is necessary to make several assumptions and specify several conditions. The assumption is made that ranging functions are complete and that a voltage of –6.3524 volts is appearing at the input to the main chassis. (R102) The instrument is entering a Measurement Cycle.

The –6.3524 volts is amplified and inverted by the Inverting Amplifier and appears at the Polarity Detector which is enabled by Gate 4 pulse. The voltage is now positive due to the action

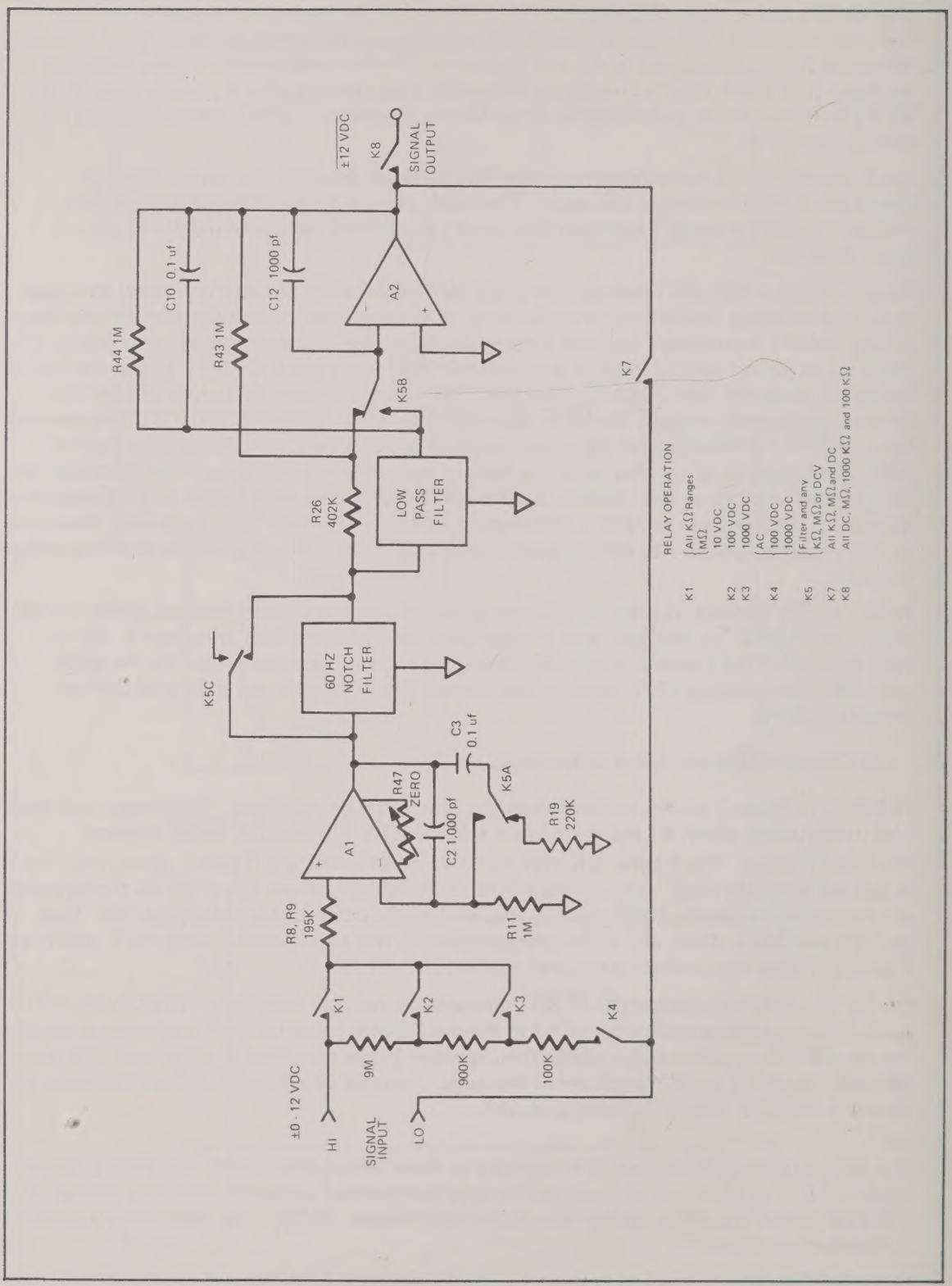


FIGURE 6. BLOCK DIAGRAM OF BUFFER

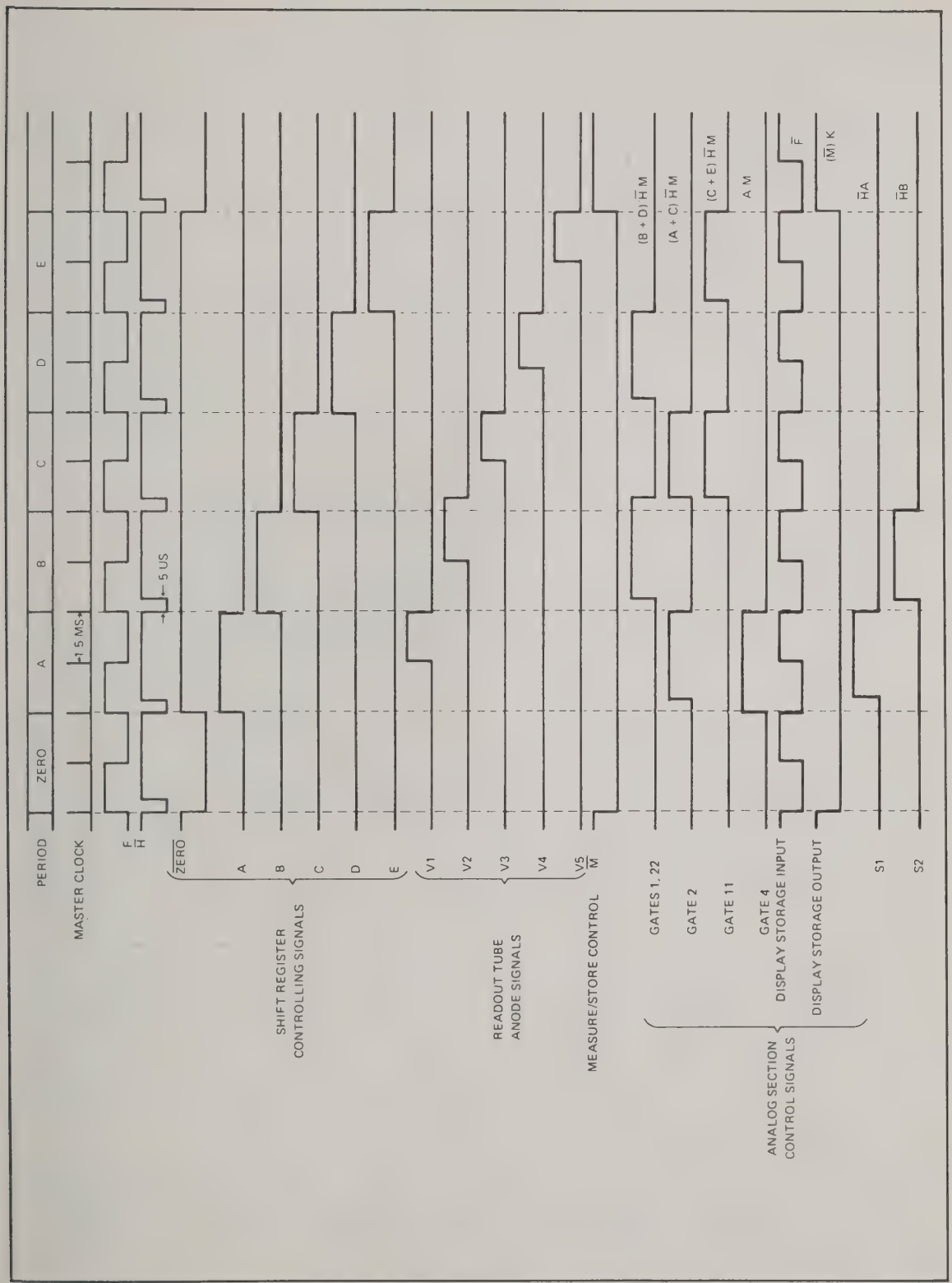


FIGURE 7. MEASUREMENT CYCLE TIME RELATIONS

of the Inverting Amplifier. The positive output to the Polarity Detector will cause the Polarity Detector to turn the plus gate Q112 on. This will cause the negative input to R102 to move directly to the input of the A-D Amplifier through R166. (In the case just taken the input to the instrument would have been positive. Had the input been negative, the Polarity Detector would have turned on the Minus gate, Q111 and the incoming signal would have been inverted by the Inverting Amplifier. This output is fed to the A-D Amplifier through R165.

NOTE: The inverting amplifier is used only when the input to the 8300A is negative.

The negative voltage appearing at the inverting input to the A-D Amplifier will cause a positive voltage to appear at its output. When the output of the A-D Amplifier exceed the 7.0 volt reference, the Analog Comparitor will produce current. This current is fed to the Current Controlled Oscillator (CCO). The Current Controlled Oscillator will produce a pulse train whose repitition rate is proportional to the current being supplied. These pulses are fed to the 16 State Binary Counter where they are translated into Binary Coded Decimal (BCD) output. The BCD output is connected to the Ladder Driver circuits and with each incremental increase of digit value the ladders will produce a current step. When the Primary Ladder has been caused to step 6 times the output from the Ladder being fed back to the input of the A-D Amplifier will cause the amplifier to satisfy itself with an output of less than 7 volts. At this time the Analog Comparitor will no longer supply current to the Current Controlled Oscillator and no further pulses will be generated. The remainder voltage that appeared at the output of the A-D Amplifier to satisfy it is now applied to capacitor C118 through Q125 which was enabled by the Gate 2 pulse (Sample and Hold)

The secondary Ladder output is fed to capacitor C110 in Display Storage. The BCD output of the 16 State Binary Counter is also fed to the Decoder Driver, where it is decimalized, which will cause ground potential to appear on the "6" line to all readout tubes. The A pulse and the F pulse are fed into the Anode Strobing Control which will cause the +190 volts to be pulsed on during the last half of the A time period, thus causing the "6" to be displayed by the first readout tube.

At the beginning of the B time period the $\overline{H}$ pulse will reset the 16 State Binary Counter. The Gate 1 & 22 pulse will enable Sample and Hold transistors Q124 and Q127. The remainder voltage stored on capacitor C108 is now applied to the input to the A-D Amplifier. The output of the amplifier will exceed 7 volts and again the Analog Comparitor will produce current, which is fed to the Current Controlled Oscillator. The oscillator pulses are counted by the 16 State Binary Counter and converted to BCD. The Ladders are caused to increase their output incrimentally with each pulse until the Primary Ladder feeds a "3" pulse back to the summing junction of the A-D Amplifier. At this time the output of the amplifier is less than 7 volts which causes the Analog Comparitor to stop the current flow to the Current Controlled Oscillator. Etc. The remainder voltage appearing at the output of the A-D Amplifier is applied to capacitor C109 in the Sample and Hold circuit through Q127. The Secondary Ladder output is stored on Display Storage capacitor C111 through Q129 and Q147.

Again the Decoder Driver has caused a ground potential to appear on all of the "3" lines to the Readout tubes and the F pulse through CR105 and the B pulse through Q34 will cause the +190 volts to be applied to the second readout tube, where the digit "3" will be displayed.

The process continues using alternately capacitors C108 and C109 in the Sample and Hold circuit to store the remainders and then reapply them to the summing junction of the A-D Amplifier. As each time period digit is developed, the Secondary Ladder stores its output on seccessive capacitors in the Display Storage capacitors C110 through C114.

It is well to remember that the above description was of a Measure Cycle. All of the digits were developed using the Sample and Hold circuit. The following description is of the Storage Cycle.

Gate pulse 4 is the primary control over the determination of whether the 8300A will enter a Measure Cycle or a Storage Cycle. If Gate 4 pulse is not present the Polarity Detector will not be activated and the instrument will continue in Storage Cycle. Gate 4 pulse is generated by Q116 and will only be present in A period when an M signal is present.

Since in this example we are entering a Storage cycle no Gate 4 signal will be present and Q146 in the Display storage will be enabled. The last Measurement Cycle left incremental voltages stored in the Display Storage capacitors C110 through C114 that correspond to the digits 63524.

During the A period Q128 and Q146 will be enabled allowing the voltage stored in C110 to be applied to the input to the A-D Amplifier. The output of the amplifier will exceed 7 volts and the Analog Comparitor will supply current to the Current Controlled Oscillator. The oscillator will generate a series of pulses causing the 16 State Binary Counter to translate the pulses into BCD output. The BCD output will cause the Ladders to switch until the Primary Ladder output satisfies the A-D Amplifier feedback. At this point in time the output from the amplifier will be below 7 volts and the Analog Comparitor will no longer supply current to the CCO. The pulses stop and the output of the Secondary Ladder will again be stored in capacitor C110 in the Display Storage circuit. The BCD 6 from the 1 6 State Binary Counter will drive the Decoder Driver which will produce a ground potential on all of the "6" leads to the readout tubes. The combination of A and F pulses will cause Q35 and Q40 to apply +190 volts to the anode of V1 which will light the "6".

During the B period, Q129 and Q147 will be enabled, applying the voltage stored in C111 to be applied to the summing junction of the A-D Amplifier. The output of the A-D Amplifier will exceed the 7.0 volt reference and the analog comparitor will supply current to the Current Controlled Oscillator. The pulses from the CCO will be counted and translated to BCD output by the 16 State Binary Counter.

The BCD output being applied to the Ladder Driver Circuits will cause the ladders to increase their outputs until the output of the Primary Ladder, which is fed back to the summing junction of the A-D Amplifier satisfies the amplifier. At this point in time the output of the amplifier will be below the 7.0 volt reference and the Analog Comparitor will no longer furnish current to the CCO and the pulses will stop. Since a "3" was digitized and stored in the Display Storage for this time period, a three from the Primary Ladder will cause the A-D Amplifier to be satisfied. The output of the Secondary Ladder will be stored in the Display Storage during the last half of the time period and the "3" will be displayed by V2 during the last half of the time period by the operation of the Anode Strobing Control.

Each increment of voltage stored in the Display Storage will be digitized and re-stored in the Display Storage circuit until all five digits have been displayed. At the end of the Storage Cycle if no Measure pulse has been generated prior to A time the 8300A will again enter a Storage Cycle. This process will repeat until a Measure pulse is generated, prior to A time and then at A time a Gate 4 pulse will be generated and the instrument will again sample the input voltage and enter a Measurement Cycle.

Refer to Figure 8 for a recap of the Measurement Mode and Storage Mode of operations.

Logic Section (Figures 7, 9, 10, 11, 12 and Schematic No. 3 sheets 1 and 2)
The Master Clock provides the timing for the entire instrument. The pulses from the flip-flop are fed to the clock input of a J-K flip-flop where the F and $\overline{F}$ pulses are generated.

The F pulse is then applied to Q1 where the $\overline{H}$ pulse is generated. (Figure 7).

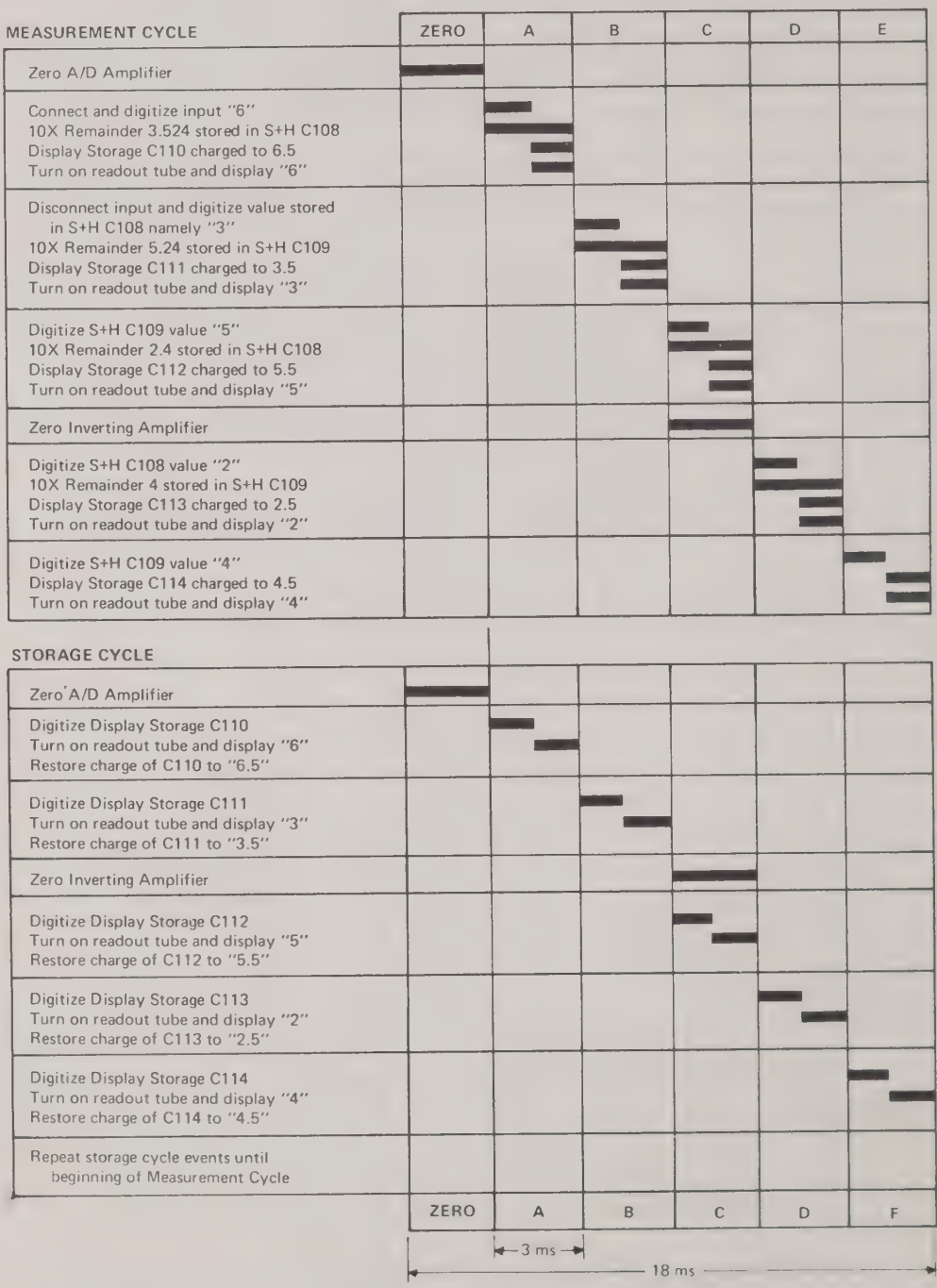

MEASUREMENT CYCLE
ZERO
A
B
C
D
E
Zero A/D Amplifier
Connect and digitize input "6"
10X Remainder 3.524 stored in S+H C108
Display Storage C110 charged to 6.5
Turn on readout tube and display "6"
Disconnect input and digitize value stored in S+H C108 namely "3"
10X Remainder 5.24 stored in S+H C109
Display Storage C111 charged to 3.5
Turn on readout tube and display "3"
Digitize S+H C109 value "5"
10X Remainder 2.4 stored in S+H C108
Display Storage C112 charged to 5.5
Turn on readout tube and display "5"
Zero Inverting Amplifier
Digitize S+H C108 value "2"
10X Remainder 4 stored in S+H C109
Display Storage C113 charged to 2.5
Turn on readout tube and display "2"
Digitize S+H C109 value "4"
Display Storage C114 charged to 4.5
Turn on readout tube and display "4"
STORAGE CYCLE
Zero A/D Amplifier
Digitize Display Storage C110
Turn on readout tube and display "6"
Restore charge of C110 to "6.5"
Digitize Display Storage C111
Turn on readout tube and display "3"
Restore charge of C111 to "3.5"
Zero Inverting Amplifier
Digitize Display Storage C112
Turn on readout tube and display "5"
Restore charge of C112 to "5.5"
Digitize Display Storage C113
Turn on readout tube and display "2"
Restore charge of C113 to "2.5"
Digitize Display Storage C114
Turn on readout tube and display "4"
Restore charge of C114 to "4.5"
Repeat storage cycle events until beginning of Measurement Cycle
ZERO
A
B
C
D
F
3 ms
18 ms

FIGURE 8.

The 6 State Shift Register (Figure 9), logic pack 4B, generate the six timing pulses used for timing in the instrument. These are the ZERO, A, B, C, D, and E pulses which are all clocked to the $\overline{H}$ pulses. This register is reset by the measure storage pulse from logic pack 16C at the end of each complete instrument cycle.

The 16 State Binary Counter (Figure 10) translates the pulses from the Current Controlled Oscillator into Binary Coded Decimal (BCD) output and controls the Ladder Switches and the Decoder Driver. It is reset at the beginning of each time period by the H pulse.

The 9's Catcher gate 9B operates from $\overline{W}$ and $\overline{Z}$ and A commands to stop the Current Controlled Oscillator.

The Conditional 11's Catcher, logic packs 8A and 19B operate to stop the 16 State Binary Counter in the A period.

The 12's Catcher operates in the A period and causes the instrument to up-range and the Over light to turn on.

Current Controlled Oscillator produces a pulse train that is proportional in repetition rate to the current being supplied. The oscillator is stopped in F time. It's output is fed to the 16 State Binary Counter to be translated into BCD output.

Analog Cycle Control provides gating functions that prevent the instrument from recycling until it completes it's present cycle, thus avoiding erroneous readings.

Manual Range Logic provides first priority of selection to the local front panel switches and provides the range commands as shown in Figure 11. Figure 12 shows the output as fed to the range flip-flop 18a and 18b.

Auto Range Logic operates when W and X from the 16 State Binary Counter and causes $\overline{UP}$ which initiates up ranging in the A period. $\overline{W}$ and $\overline{X}$ and $\overline{Y}$ and $\overline{Z}$ (zero) result in a $\overline{DN}$ signal which initiates down ranging in the A period. In addition when no Filter selection is made the instrument requires a settling time of about 10 ms. This is provided by R40 shunted by R41. When the Filter is selected R40 provides about 230 ms of delay for settling time.

E. Display (Schematic No. 4)

Display Circuits consist of the Function Lights, which are 5 volt lamps operated by the logic controls in the instrument and the relays and associated circuitry.

The Anode Strobing Control provides +190 volts to the readout tubes during the last half of each time period and lights each lamp in coordination with the proper time period.

Decoder Driver accepts the BCD output from the 16 State Binary Counter and translates it into decimal output, grounding the appropriate line to the readout tubes so that the tube will light when the +190 volts is applied by the Anode Strobing Control. Q41 operates the first readout tube whenever the count in A period reaches ten.

F. AC CONVERTER THEORY (Figure 13 and Schematic No. 6)

The AC Converter option for the 8300A converts input AC voltages, in four ranges, to DC for measurement by the A-D Converter. The output of the Converter is 0 to 12 VDC , which represents full scale.

PERIOD	SIX STATE SHIFT REGISTER				
	1A	1B	2C	2D	3E
ZERO	0	0	0	0	0
A	1	0	0	0	0
B	0	1	0	0	0
C	0	0	1	0	0
D	0	0	0	1	0
E	0	0	0	0	1

Figure 9.

RANGE	FLIP-FLOP	
	18a	18b
1	0	0
10	0	1
100	1	0
1000	1	1

Figure 12.

CCO PULSE COUNT	16 STATE BINARY COUNTER			
	7W	7X	6Y	6Z
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0

Figure 10.

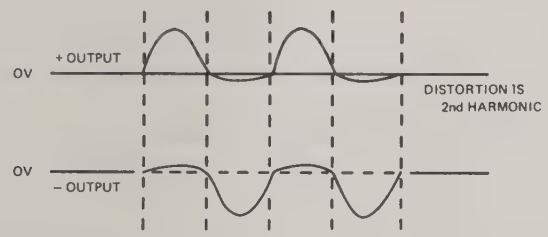
NOR GATES	RANGE									
	VAC & KΩ				VDC			MVDC		MΩ
	1	10	100	1000	10	100	1000	100	1000	10
12B	1	0	0	0	0	0	0	0	0	0
10D	0	1	0	0	1	0	0	0	0	0
10B	0	0	1	0	0	1	0	1	0	0
10C	0	0	0	1	0	0	1	0	1	0

Figure 11.

Zero adjust for the AC Option is located on the Buffer Board and is accessable from the front panel. Calibration of the assembly is made in the factory prior to shipment and the board may be placed in an instrument, the zero adjustment made and calibration checked. It should not be necessary to recalibrate the option after installation.

The block daigram, (Figure 13) is divided into two major parts. A wide band operational rectifier circuit where the ranging is accomplished and a DC difference (or subtracting) amplifier-intergrator where the rectifier output is filtered and amplified. The DC amplifier also provides the low source impedance required by the A-D Converter.

The operational rectifier circuit consists of an inverting transconductance amplifier and load resistor with feedback around them providing a loop gain of about 5×10^3 at mid band. The feedback is changed for ranging with reed relay switches. The input resistor is 1.11 megohms. This value shunted by the 10 megohm DC input divider is 1 megohm at the 8300A input. Q1 is a FET used as a source follower and Q2 provides a low impedance guard voltage which is used to bootstrap most of the capacity that otherwise would appear from the FET gate to common. The first two differential pairs are in a dual inline package. They and Q4 and Q5 develop the gain. Q3 and Q6 are current sources with such values that clipping due to overload is symmetrical. Changes in capacitor charges will be small and amplifier recovery time minimized. Q7 compensates for capacitance losses in the diodes at low levels. A symmetrical half wave rectifier placed between the amplifier and load resistor develops equal (+) and (—) DC voltages proportional to the amplifier output current. At full scale this current is near 2 ma. The two outputs have the following wave forms.



The DC difference amplifier-integrator filters the waveform and amplifies the DC difference between them by about 10 times for measurement by the A-D Converter. Three section filtering, which cannot be observed on the readout when the input voltage is at full scale and above 100 Hz. Below 100 Hz a few digits respond to the ripple. At 50 Hz the readout excursions do not exceed ±.01% of reading and at 30 Hz are within ±.05% of reading. Q9 is a dual FET which is used for the input of the low drift DC amplifier. Further gain for the DC amplifier is developed by a monolithic operational amplifier to produce a total loop gain at DC of about 5×10^5.

G. MILLIVOLT/OHMS CONVERTER THEORY (Figure 14, 15 and Schematic No. 7)

As the name implies, the Millivolt/Ohms Converter performs two functions. The use of the converter in the 8300A allows measurement of resistance over five ranges and provides two DC voltage ranges in addition to the three ranges offered by the basic instrument. The five resistance ranges are 1 KΩ, 100 KΩ, 1000 KΩ and 10 MΩ. The two additional DC voltage ranges are 100 mv and 100 mv. As with the basic instrument, the above ranges have a 20% over-range capability. Thus the 1 KΩ range will accurately read to 1.19999 KΩ.

This converter can be thought of as two converters. One converter is a chopper amplifier which provides a DC amplification of an unknown voltage prior to A-D Conversion. Signal gain is necessary if a 100 mv signal on the 100 mv range is to provide a corresponding 10V DC signal into the A-D Converter.

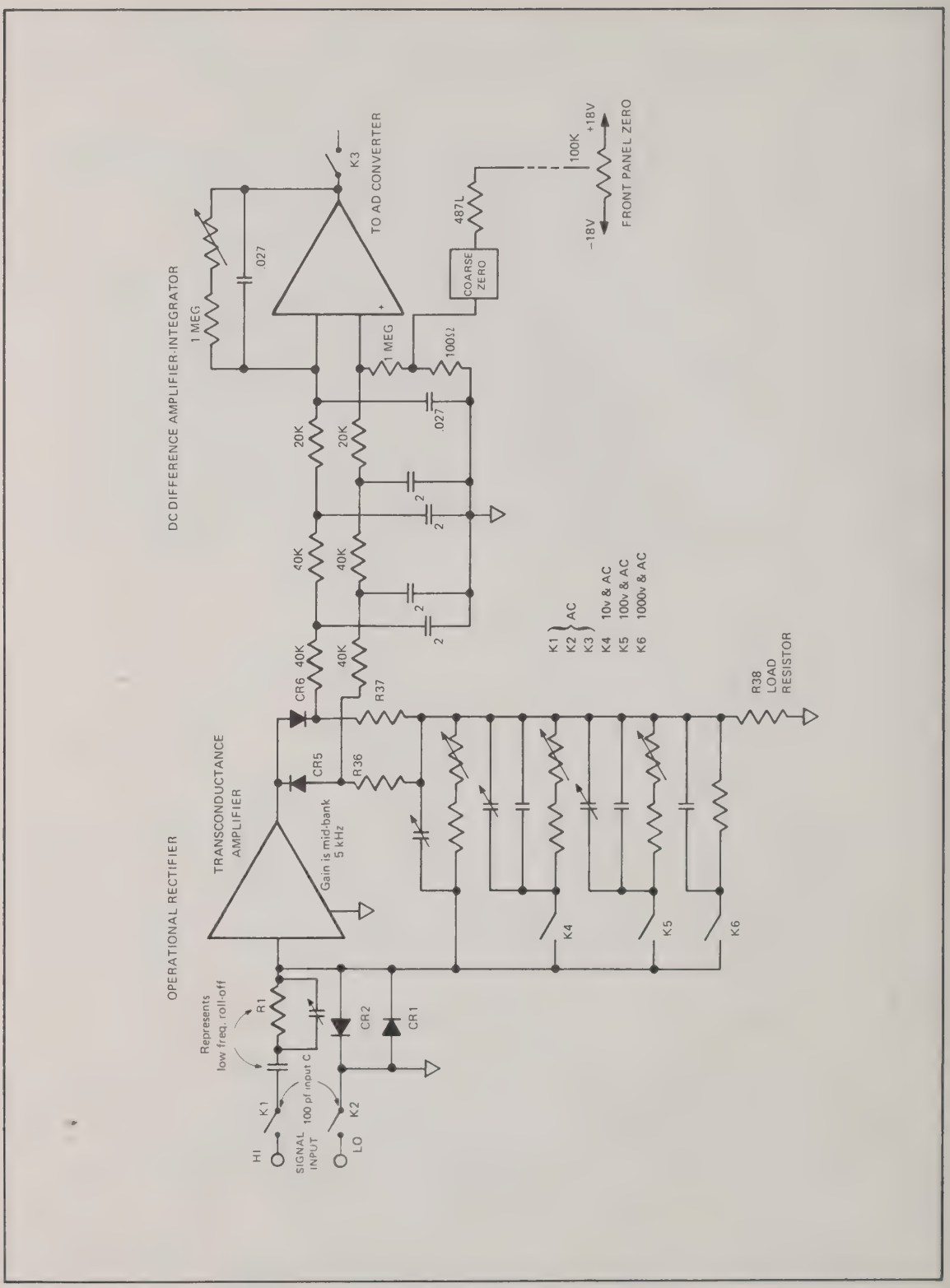


FIGURE 13. BLOCK DIAGRAM AC CONVERTER

The other converter in the Millivolt/Ohms Converter is a precision current ladder which, in conjunction with the Buffer amplifier, provides a known current through the resistor to be measured. Refering to Figure 14, a MOSFET chopper is used across the summing junctions of an operational amplifier. The signal developed due to the chopping action is amplified and presented through a capacitor to a half-wave synchronous demodulator. The Demodulator output is sent to a high gain (at DC) operational amplifier connected as an integrator. The integrator output is brought to the MOSFET chopper in a manner to insure negative feed-back. An input RC network provides input filtering to prevent beat frequency products at the amplifier output and balanced AC impedances for the chopper.

The use of the MOSFET chopper as shown allows the spike developed due to capacitive coupling from gate drive to channel to become a common mode signal for a high common mode rejection operational amplifier. Balanced AC impedances at the chopper provide cancellation effect of the offset current and voltage due to the capacitive spike. The new result is a chopper amplifier capable of operating at a fairly high frequency with small voltage and current offsets, and with spikes of low enough value to keep the AC amplifier from saturating. The above operation is achieved without large adjustments for spike compensation.

The overall millivolt amplifier can be considered to be a high DC gain operational amplifier utilizing potentiometric feedback to provide programmed gains of x10 or x100 and very high input impedance at DC. The A-D Converter follows the millivolt converter to provide digitization of the amplified analog representation of the input signal to the millivolt converter.

The current ladder is connected to the Buffer and the millivolt converter as shown in Figure 15. The inverting terminal of the Buffer amplifier is held very near analog common by the feedback connection of the unknown resistance. Because the inverting terminal is held near ground, and because the input current to the Buffer is small, the current through the unknown resistor is set by the reference voltage (7 volts) and the resistor selected by the range command. For the three upper KΩ ranges, the output of the buffer is presented to the A-D Converter. Thus since the A-D Converter digitizes 11.9999 as full scale, then that voltage must represent full scale on the KΩ ranges. Simple arithmetic shows us that the sampling currents for the three ranges to be 1 ua, 10 ua, and 100 ua respectively.

For the 1 KΩ and the 10 KΩ range, smaller full scale voltages are used in order to keep load dissipation down. Thus, on these two ranges, the millivolt converter is used to amplify the voltage across the unknown resistor and present the amplified voltage to the A-D Converter.

In addition to providing smaller full scale impressed voltages in the lower two resistance ranges, the use of the millivolt converter allows a "modified four terminal" resistance measurement to be made. The term "modified four terminal" is used because the technique employed requires a small current in one of the sense lines that would not be present in a true four terminal resistance measurement. The sense current magnitude is determined by the voltage impressed on the resistor to be measured divided by R_i. By example, if the sense line resistance is 10Ω, then the error due to the sense current can be computed roughly as follows:

$$\text{Error} = \frac{10\Omega}{R_i} = \frac{100\Omega}{1000\Omega} = 10^{-4} \text{ or } 100 \text{ ppm of reading.}$$

If a two terminal reading were made at the 1 KΩ level with a 10Ω resistance in the hook-up wires, the error would be about 10,000 ppm. The improvement in performance using a "modified four terminal" measurement is obvious.

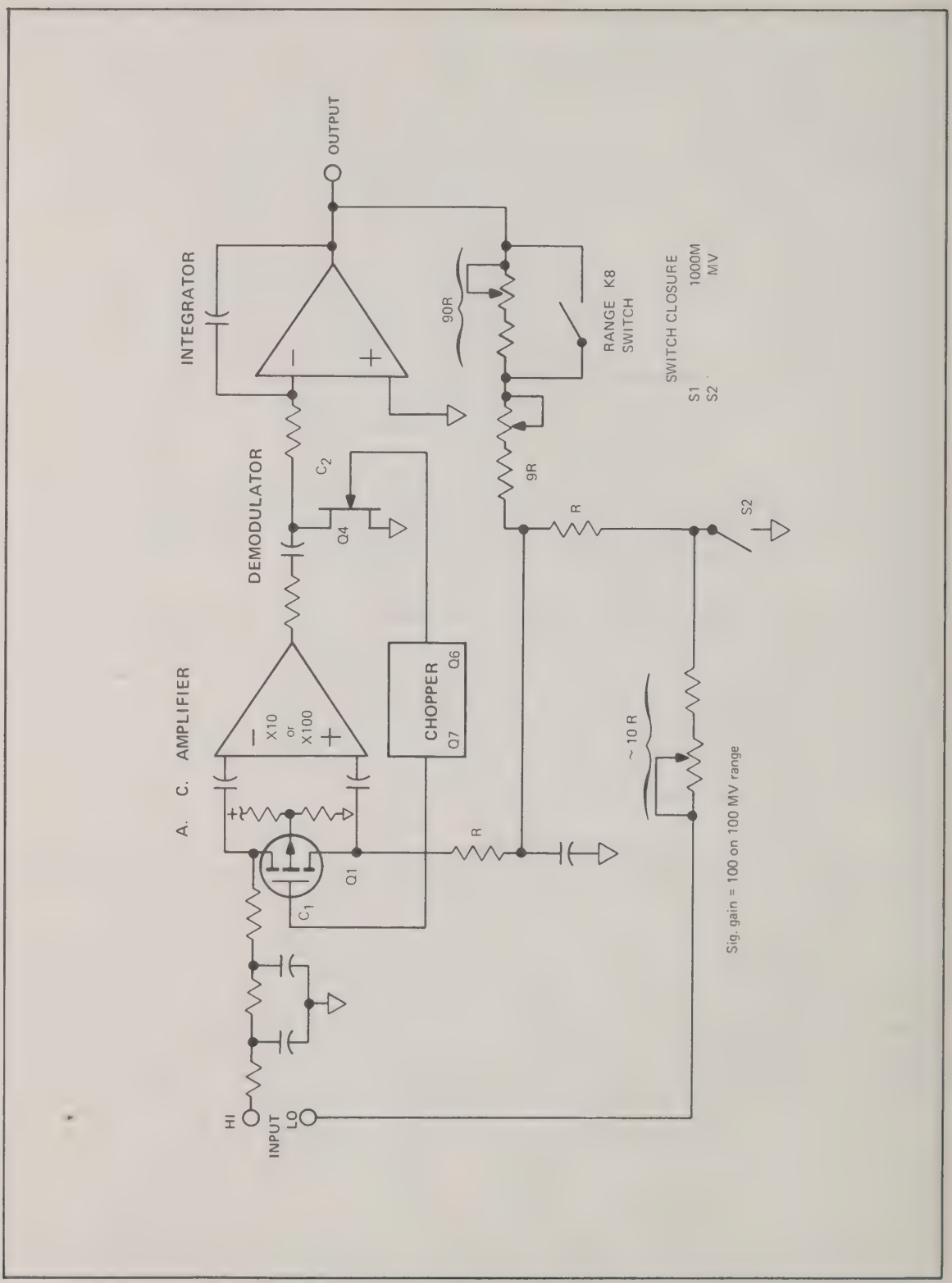
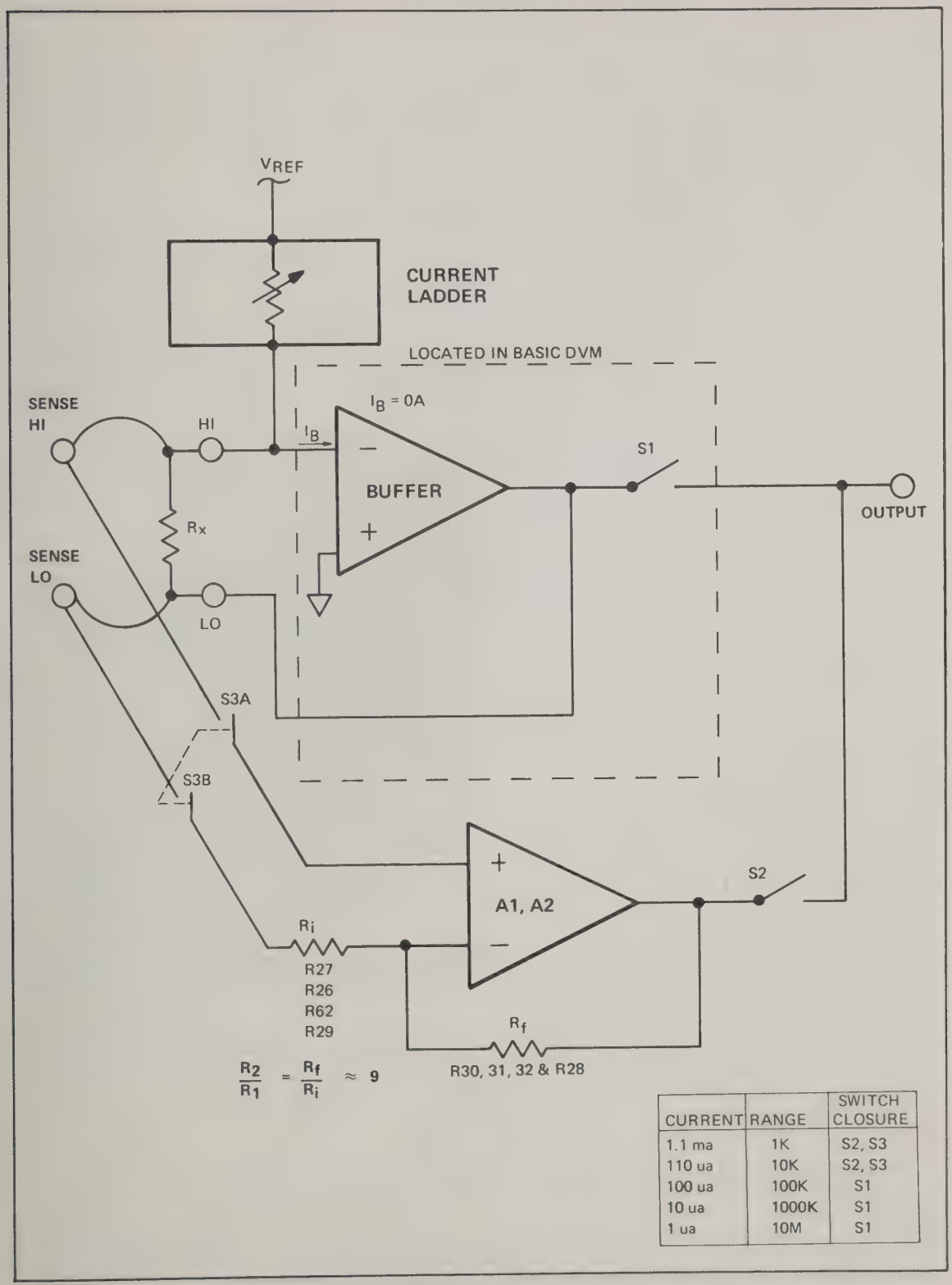


FIGURE 14. BLOCK DIAGRAM OF MILLIVOLT CONVERTER



CURRENT	RANGE	SWITCH CLOSURE
1.1 ma	1K	S2, S3
110 ua	10K	S2, S3
100 ua	100K	S1
10 ua	1000K	S1
1 ua	10M	S1

FIGURE 15. BLOCK DIAGRAM OF OHM CONVERTER

H. EXTERNAL REFERENCE THEORY (Figure 16, 17, 18, 19 and Schematic No. 10)

The 8300A input terminal for VDC measurements is the input to the A-D Converter and therefore, will have a maximum voltage of ±12v with respect to the instrument common, Figure 16. Since it may be necessary to connect the common of the input to the common of External Reference input and the External Reference output common is instrument common, a means of isolating the commons becomes necessary.

Refer to Figure 17. Switches S1 and S2 are arranged so that when one set is closed, the other is open. S1 is closing during a non-critical (the A-D ZERO time) portion of the measurement cycle and allowed to charge to the voltage, E_R. When S2 is closed, the output of A_1 goes to E_R satisfying the voltage follower.

Refering to the circuit schematic, A2 is the S1 of the block diagram, Q4 and Q5 the switch, S2. A matched pair of J-FETS followed by a monolithic amplifier made up the high input impedance voltage follower. Q8 and R17 is a constant current source for the J-FET amplifiers. Frequency compensation is provided by the C4, C5 and C6.

The reference voltage is sensed through R18 from the A-D Amplifier board compensating for line drops. Low sense (Reference Common) also comes from the main board. CR7 and CR8 provide feedback to the voltage follower when the reed relay, S1 is open, keeping the amplifier output within 0.5v of the voltage of C8 to control the gate drive for Q4.

C7 forms an RC filter with the input driver giving improved noise performance. C9 provides an input impedance to the voltage follower during the time the FET switches, Q5 and Q6 are open.

Q1 and Q2 are gate drivers for the J-FET switches. Using the reference voltage for the collector supply of Q2 assures that the gate signal of Q4 never goes positive with respect to its terminal. The gate of Q5 is clamped to within .2v of common by diode CR6. R13 limits the current through CR6. C2 compensates for the capacity of CR6.

A voltage of as much as ±12.0v with respect to reference common will appear at the low terminal of EX REF input when the EX REF common is tied to the instrument input common.

A schematic showing the voltage distribution is shown in Figure 25. The MOS FET's used are P-channel enhancement mode devices. A negative gate voltage of 10v or more is needed to insure that the transistor is on. 0v or a positive gate voltage turns the transistor off. Refering to Fig.18, the upper switch needs a minimum of −15v to turn on and a maximum of 19v to turn off. The bottom switch needs a minimum of −22v to turn on and a maximum of 12v to turn off.

The MOS FET gate driver is redrawn in Figure 19 showing the peak voltages. When the transistor is saturated, CR1 is back biased. When the transistor is cutoff, C3 charges to 8v because of the 12v drop across the zener. This voltage subtracts from the collector voltage giving the voltage shown.

When the EXT REF control line is 5v (the EXT REF button pushed) −18v is applied to the local Disable line with Q10 and Q12.

Input protection is provided with CR4, CR5 and R12.

III. TROUBLESHOOTING AND ANALYSIS (Figure 20. 21, 22, and 23)

1. The following is a list of recommended test equipment that is required to test and calibrate the 8300A. If the recommended equipment is not available, other equipment which meets the required specifications may be used.

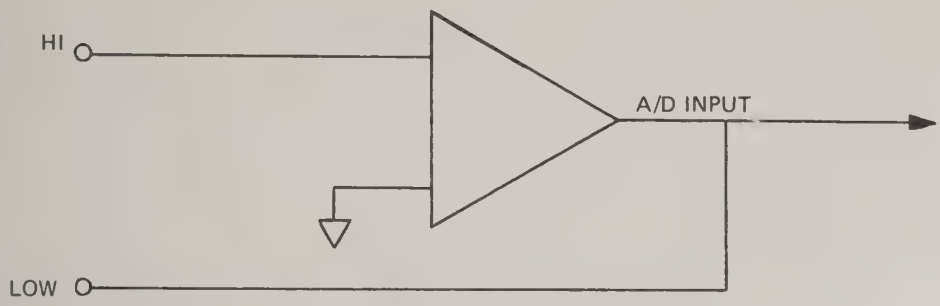


FIGURE 16.

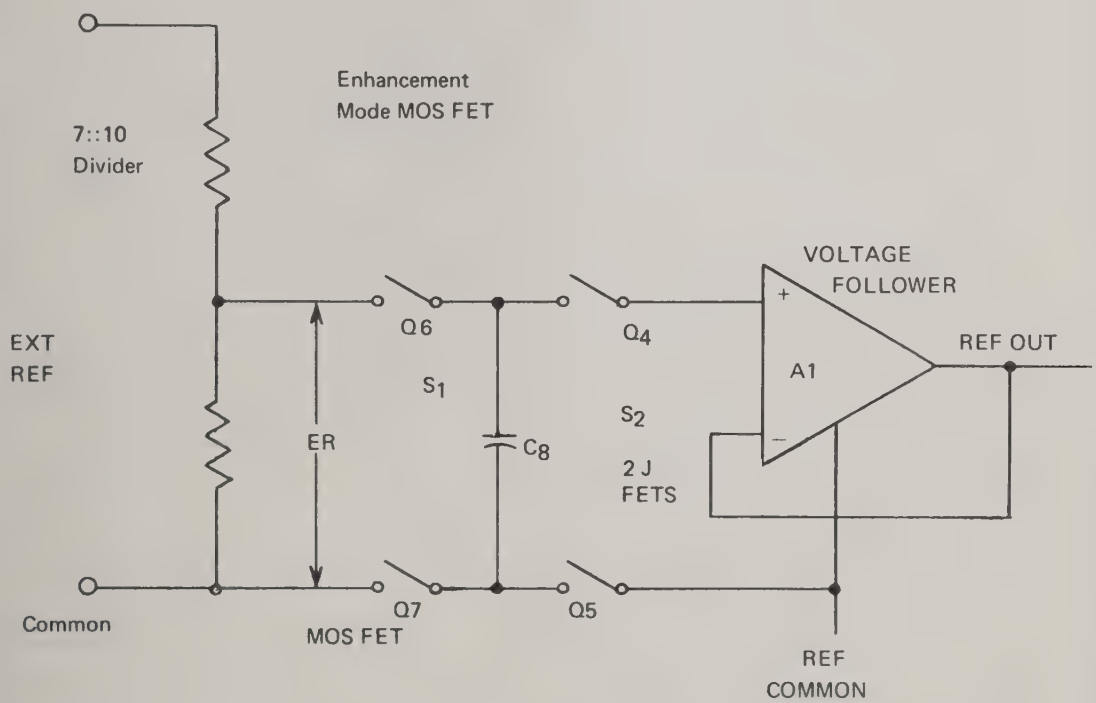


FIGURE 17.

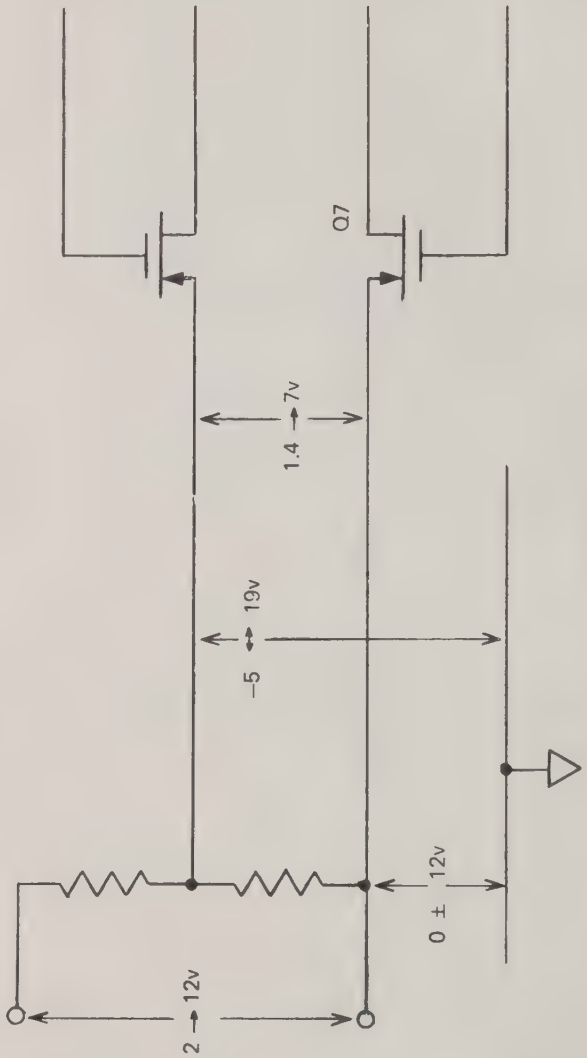


FIGURE 18.

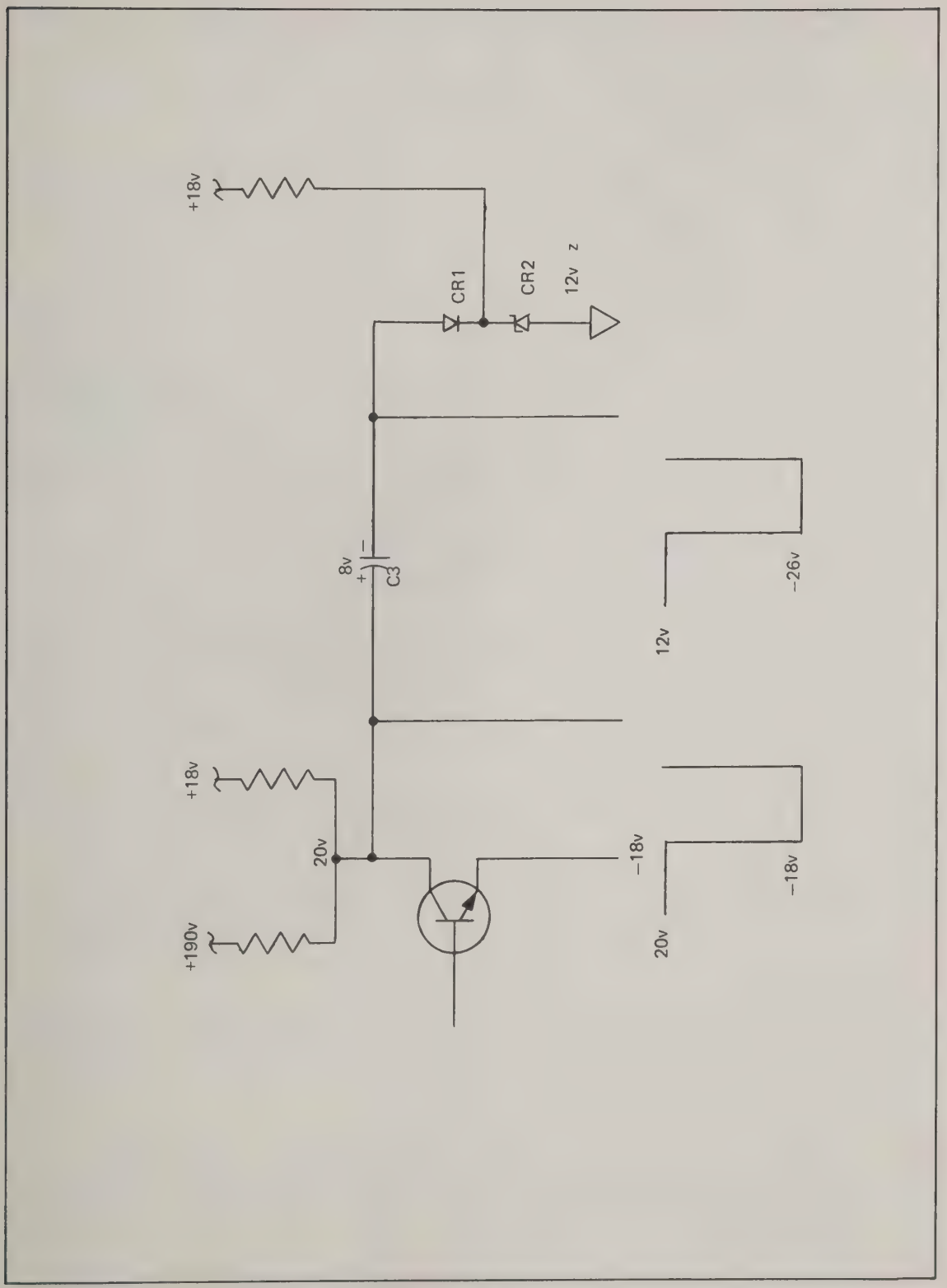


FIGURE 19.

EQUIPMENT NOMENCLATURE	RECOMMENDED EQUIPMENT
Oscilloscope	Tektronix Model 547
Oscilloscope Plug-In	Tektronix Model 1A1
Oscilloscope Probes	Tektronix Model P6010
DC Voltage Source	Fluke Model 343A DC Voltage Calibrator
AC Voltage Source	HP Model 745A
Differential Voltmeter	Fluke Model 885A

2. An excellent source of synchronization for the Oscilloscope may be obtained by using the $\overline{\text{ZERO}}$ signal that is available at TP4 or TP108. By proper adjustment of the horizontal trace time it is possible to see all of the other timing pulses in their proper relationship.

3. With the covers and shields removed it is reasonable to expect to see more noise in the output as the 8300A is quite sensitive to interference when these protections are removed.

4. Figure 20 gives the general location of the various sections of the instrument.

5. Figure 21 locates the various test points (TP) and is a guide to the location and index of the logic packs.

6. All voltage measurements and pulse observations should be made with reference to the instrument signal ground which is available at TP3 and TP109.

7. Figure 22 gives a step by step procedure for troubleshooting the Display section of the 8300A.

8. Figure 23 gives an excellent step by step procedure for troubleshooting the analog circuitry.

9. Many cases of trouble can be analized from the operation and readout observations of the instrument. As examples the following are presented:

   a. Readout is in error only in the negative polarity.

      It is reasonable to assume that the trouble is located in either the polarity FET switch or in the Inverting Amplifier since these paths are utilized only in the negative polarity.

   b. More than one digit displayed in the readout tubes.

      The Decoder Driver is the most likely source of this trouble. If ground potential is supplied to more than one of the decimal lines to the readout tubes, multiple numbers will light. There remains the possibility that the Anode Strobing circuits are malfunctioning.

   c. Only the first digit is displayed, all others read 0.

      It is reasonable to assume that the remainders are not being stored in the Sample and Hold circuitry. This can be caused by a failure in the FET switches or a short in the storage capacitors. It is also possible that two significant digits will be developed and displayed.

   d. First digit reads higher than the input voltage and all other digits read 0.

      Count the pulses from the Current Controlled Oscillator. If correct check the BCD

output of the A4 Counter. If the BCD output is correct the Ladder output voltage could be too high.

e. A large signal of either polarity is needed to cause a reading of other than 0.0000.

The A-D Auto Zeroing circuit, Q117 and Q118 should be checked.

f. None of the readout tubes lighted.

Check the +5 and the +190 volt supplied.

10. The basic instrument may be checked by applying a 0 to 12 volt DC signal at the input to the Inverting Amplifier. This should cause the instrument to display the voltage applied.

11. By applying a jumper between TP6 and TP201 the instrument can be made to sample continuiously. This procedure can be used to locate trouble in the Storage circuitry.

12. The logic section of the instrument can be broken up into several independent sections for trouble analysis as follows:

a. Master Clock

Check the output of Q45, then look for the F, $\overline{H}$ and $\overline{ZERO}$ pulses.

b. Six State Shift Register.

Check for the presence of the A, B, C, D, and E pulses and their inversions.

c. Check the output of the Current Controlled Oscillator and the BCD output of the 16 State Binary Counter.

d. Display readout tubes.

Anodes and Anode Strobing circuitry.
Cathode circuits including the Decoder Driver.
Decimal lines.

e. Function Indicators.

+5 volt incandescent lights and associated circuitry.

f. Sample Oscillator should be checked for output.

g. Figures C through G and the Picture waveforms attached will be of additional assistance in locating troubles.

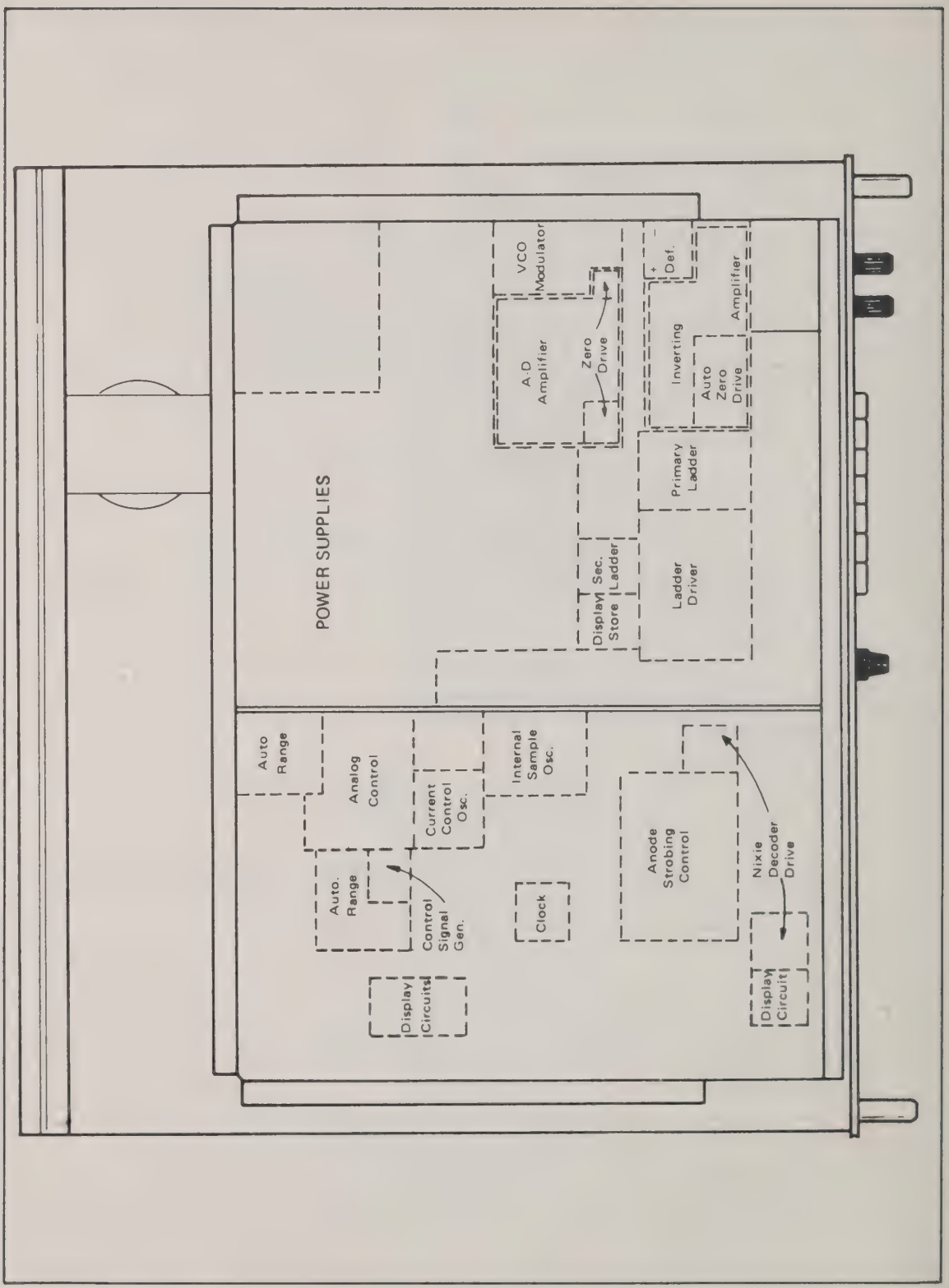

POWER SUPPLIES
VCO Modulator
A-D Amplifier
Zero Drive
+ - Def. Amplifier
Inverting
Auto Zero Drive
Primary Ladder
Ladder Driver
Display Sec. Store Ladder
Auto Range
Analog Control
Current Control Osc.
Internal Sample Osc.
Auto. Range
Control Signal Gen.
Clock
Anode Strobing Control
Nixie Decoder Drive
Display Circuits
Display Circuits

FIGURE 20.

FUNCTION VDC
INPUT ZERO VOLTS
CONDITIONS
RESULT
CORRECTIVE ACTION
ONLY ONE READ-OUT TUBE LIGHTS AND IT GLOWS BRIGHTLY
READOUT TUBES AND FUNCTION/STATUS INDICATORS BLANK
MORE THAN ONE BUT NOT ALL READOUT TUBES LIGHT
CHECK FOR PRESENCE OF ZERO SIGNAL
CHECK +5 AND +190 VOLT SUPPLIES
CHECK 1 TO 5 OFF-TO-ON RATIO OF ZERO SIGNAL
ZERO SIGNAL NOT PRESENT
RATIO NOT CORRECT
CHECK FOR PRESENCE OF H SIGNAL
CHECK FOR PRESENCE OF F SIGNAL
CHECK 6-STATE SHIFT REGISTER
CHECK FOR PRESENCE OF SIGNAL AT DARK TUBES ANODES

FIGURE 21.

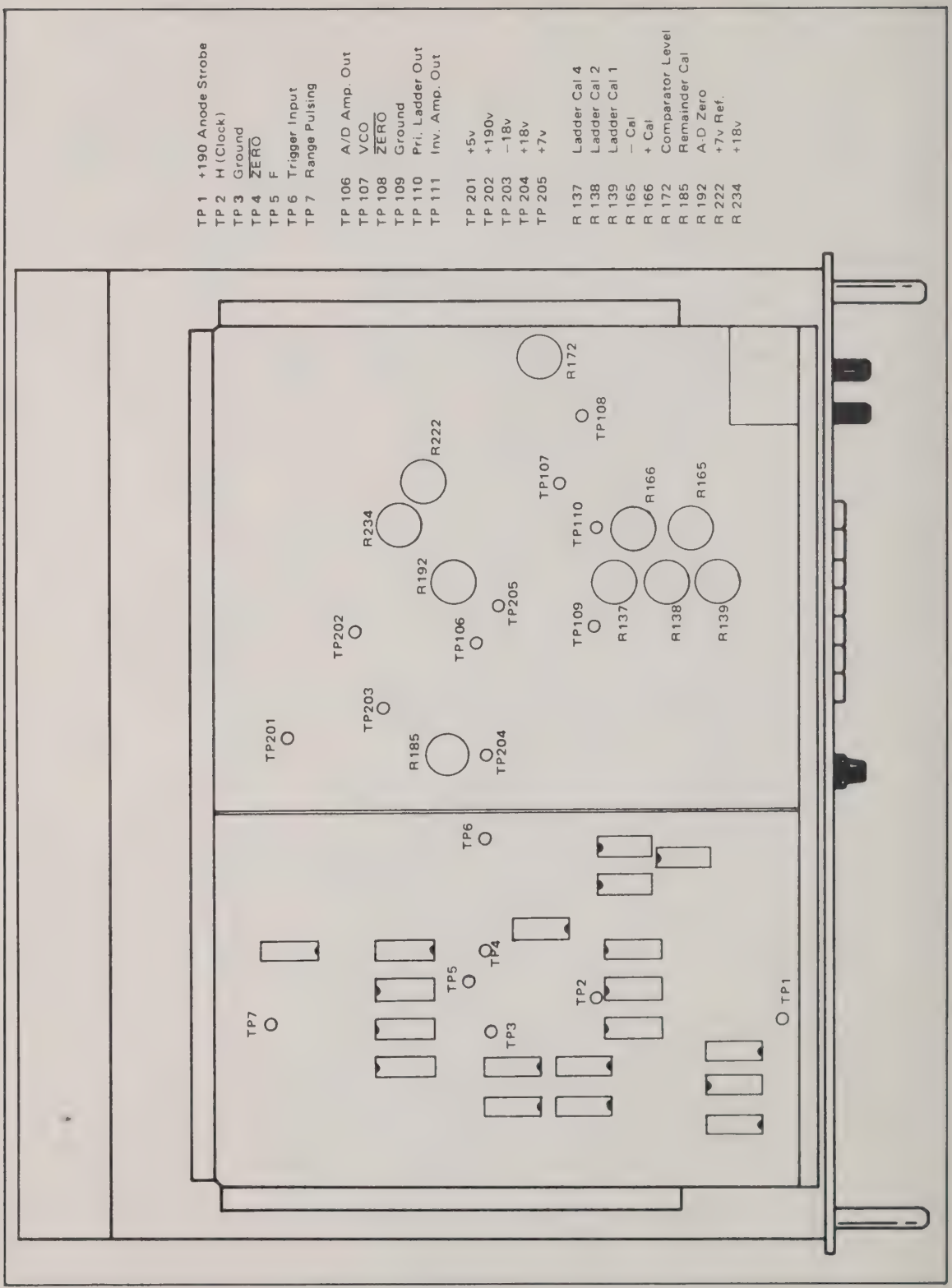

TP 1 +190 Anode Strobe
TP 2 H (Clock)
TP 3 Ground
TP 4 ZERO
TP 5 F
TP 6 Trigger Input
TP 7 Range Pulsing
TP 106 A/D Amp. Out
TP 107 VCO
TP 108 ZERO
TP 109 Ground
TP 110 Pri. Ladder Out
TP 111 Inv. Amp. Out
TP 201 +5v
TP 202 +190v
TP 203 −18v
TP 204 +18v
TP 205 +7v
R 137 Ladder Cal 4
R 138 Ladder Cal 2
R 139 Ladder Cal 1
R 165 − Cal
R 166 + Cal
R 172 Comparator Level
R 185 Remainder Cal
R 192 A-D Zero
R 222 +7v Ref.
R 234 +18v
TP7
TP3
TP5
TP4
TP6
TP2
TP1
TP201
TP203
R185
TP204
TP202
R234
R192
TP106
TP205
R222
TP109
R137
TP110
R166
R138
R165
R139
TP107
TP108
R172

FIGURE 22.

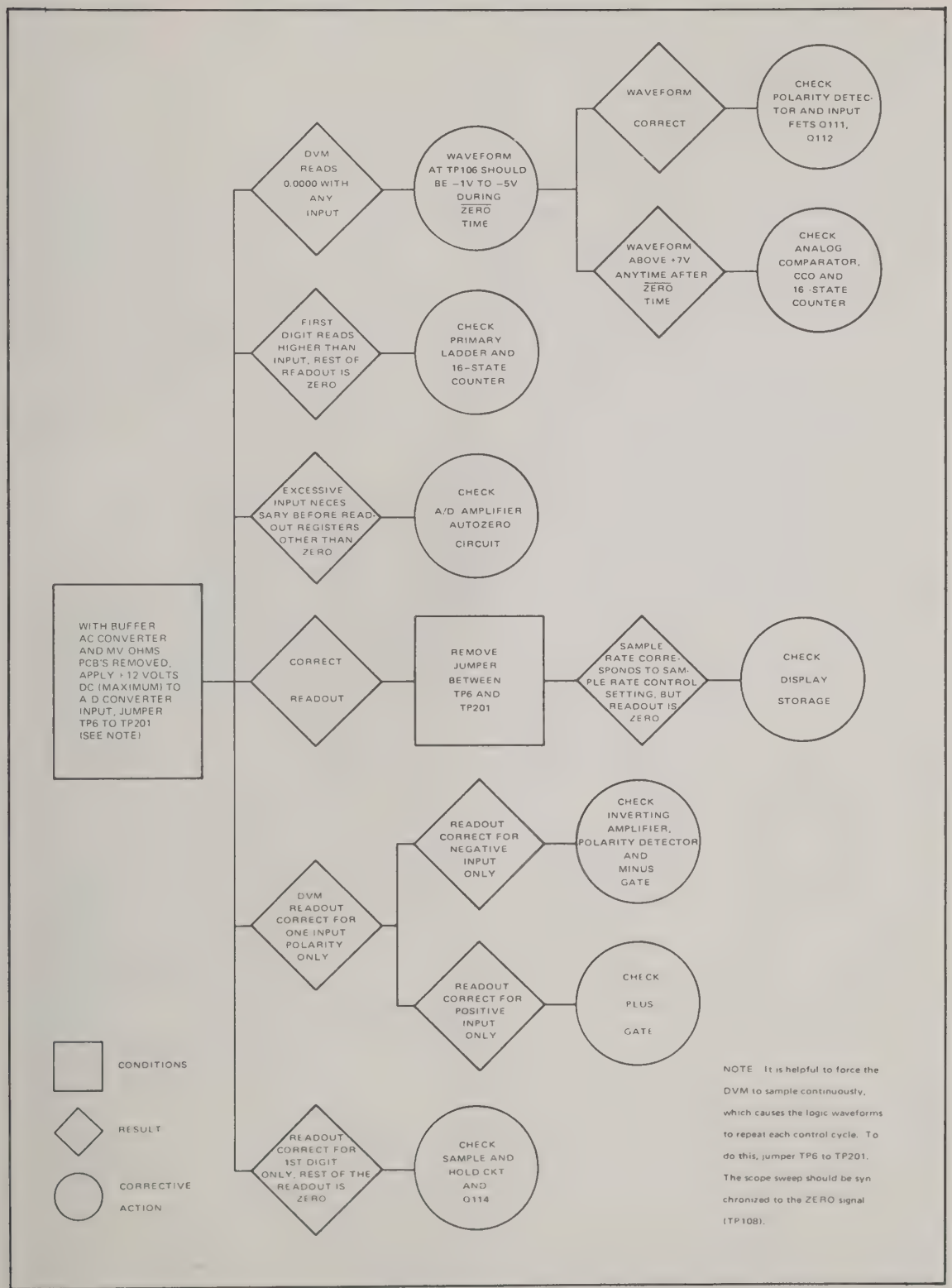
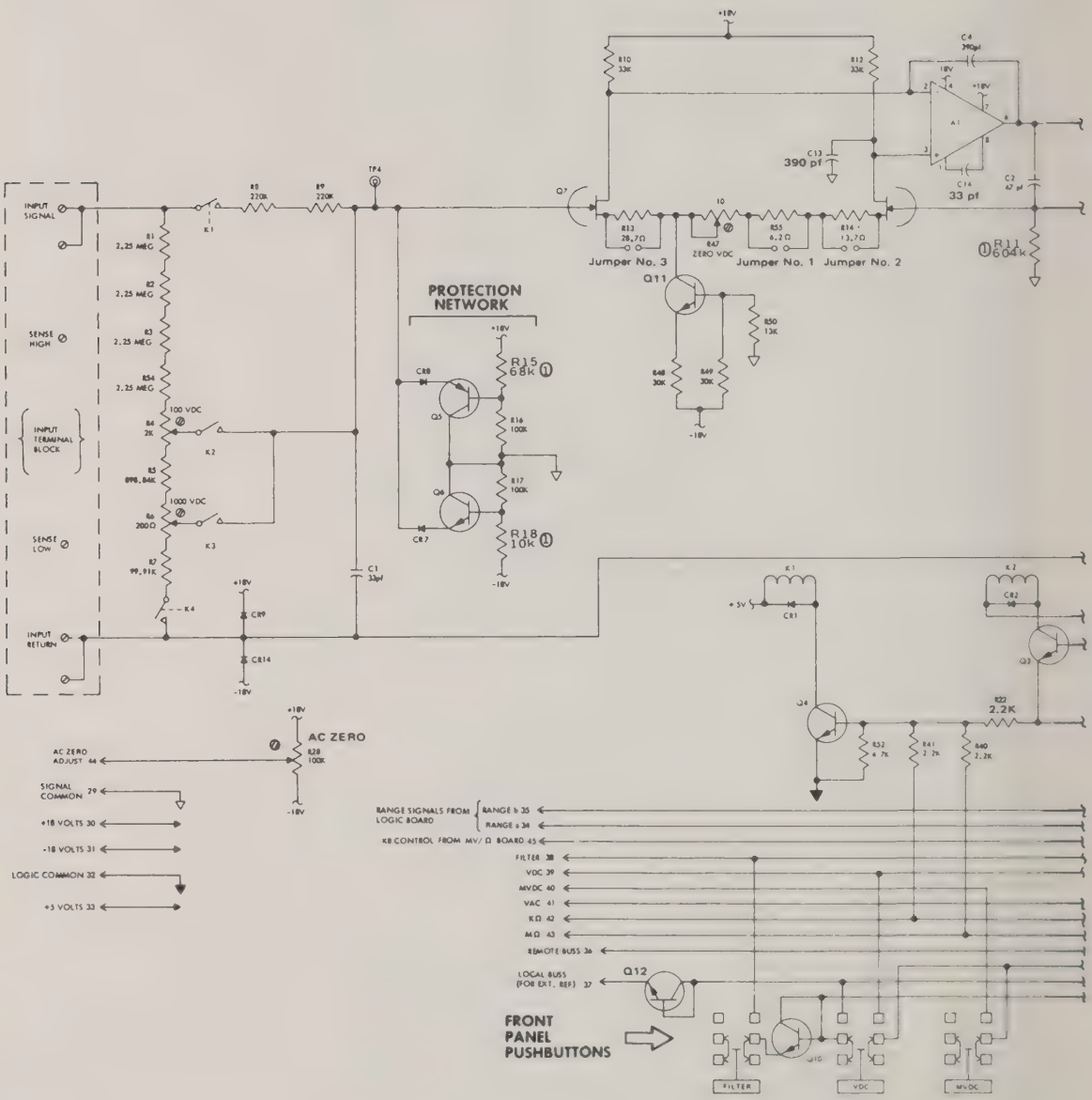
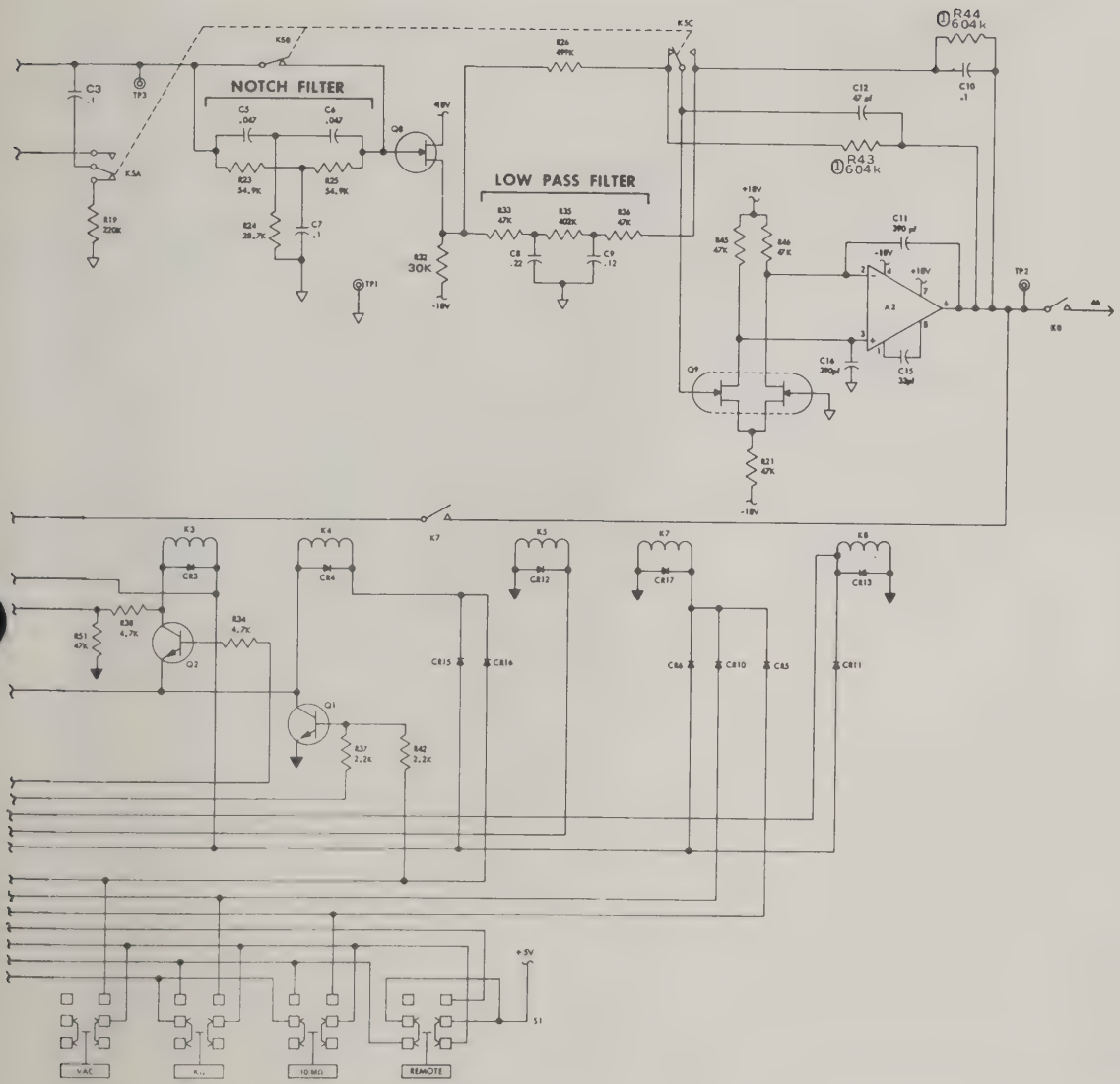

WITH BUFFER AC CONVERTER AND MV OHMS PCB'S REMOVED, APPLY +12 VOLTS DC (MAXIMUM) TO A-D CONVERTER INPUT, JUMPER TP6 TO TP201 (SEE NOTE)
DVM READS 0.0000 WITH ANY INPUT
WAVEFORM AT TP106 SHOULD BE −1V TO −5V DURING ZERO TIME
WAVEFORM CORRECT
CHECK POLARITY DETECTOR AND INPUT FETS Q111, Q112
WAVEFORM ABOVE +7V ANYTIME AFTER ZERO TIME
CHECK ANALOG COMPARATOR, CCO AND 16-STATE COUNTER
FIRST DIGIT READS HIGHER THAN INPUT, REST OF READOUT IS ZERO
CHECK PRIMARY LADDER AND 16-STATE COUNTER
EXCESSIVE INPUT NECESSARY BEFORE READOUT REGISTERS OTHER THAN ZERO
CHECK A/D AMPLIFIER AUTOZERO CIRCUIT
CORRECT READOUT
REMOVE JUMPER BETWEEN TP6 AND TP201
SAMPLE RATE CORRESPONDS TO SAMPLE RATE CONTROL SETTING, BUT READOUT IS ZERO
CHECK DISPLAY STORAGE
DVM READOUT CORRECT FOR ONE INPUT POLARITY ONLY
READOUT CORRECT FOR NEGATIVE INPUT ONLY
CHECK INVERTING AMPLIFIER, POLARITY DETECTOR AND MINUS GATE
READOUT CORRECT FOR POSITIVE INPUT ONLY
CHECK PLUS GATE
READOUT CORRECT FOR 1ST DIGIT ONLY, REST OF THE READOUT IS ZERO
CHECK SAMPLE AND HOLD CKT AND Q114
CONDITIONS
RESULT
CORRECTIVE ACTION
NOTE It is helpful to force the DVM to sample continuously, which causes the logic waveforms to repeat each control cycle. To do this, jumper TP6 to TP201. The scope sweep should be synchronized to the ZERO signal (TP108).

FIGURE 23.


INPUT SIGNAL
SENSE HIGH
INPUT TERMINAL BLOCK
SENSE LOW
INPUT RETURN
R1 2.25 MEG
R2 2.25 MEG
R3 2.25 MEG
R54 2.25 MEG
100 VDC
1000 VDC
K1
K2
K3
K4
R8 220K
R9 220K
TP4
C1 33pf
+18V
-18V
CR9
CR14
PROTECTION NETWORK
R15 68K
R16 100K
R17 100K
R18 10K
CR8
CR7
Q5
Q6
Q7
Q11
R10 33K
R12 33K
C13 390 pf
C14 33 pf
C4 390pf
C2 47 pf
R13 28.7Ω
R47 ZERO VDC
R55 6.2Ω
R14 13.7Ω
Jumper No. 3
Jumper No. 1
Jumper No. 2
R11 604K
R50 13K
R48 30K
R49 30K
AC ZERO
R20 100K
AC ZERO ADJUST 44
SIGNAL COMMON 29
+18 VOLTS 30
-18 VOLTS 31
LOGIC COMMON 32
+5 VOLTS 33
+5V
CR1
CR2
Q3
Q4
R22 2.2K
R52 4.7K
R41 2.2K
R40 2.2K
RANGE SIGNALS FROM LOGIC BOARD
RANGE b 35
RANGE a 34
KB CONTROL FROM MV/Ω BOARD 45
FILTER 38
VDC 39
MVDC 40
VAC 41
KΩ 42
MΩ 43
REMOTE BUSS 36
LOCAL BUSS (FOR EXT. REF) 37
Q12
FRONT PANEL PUSHBUTTONS
FILTER
VDC
MVDC

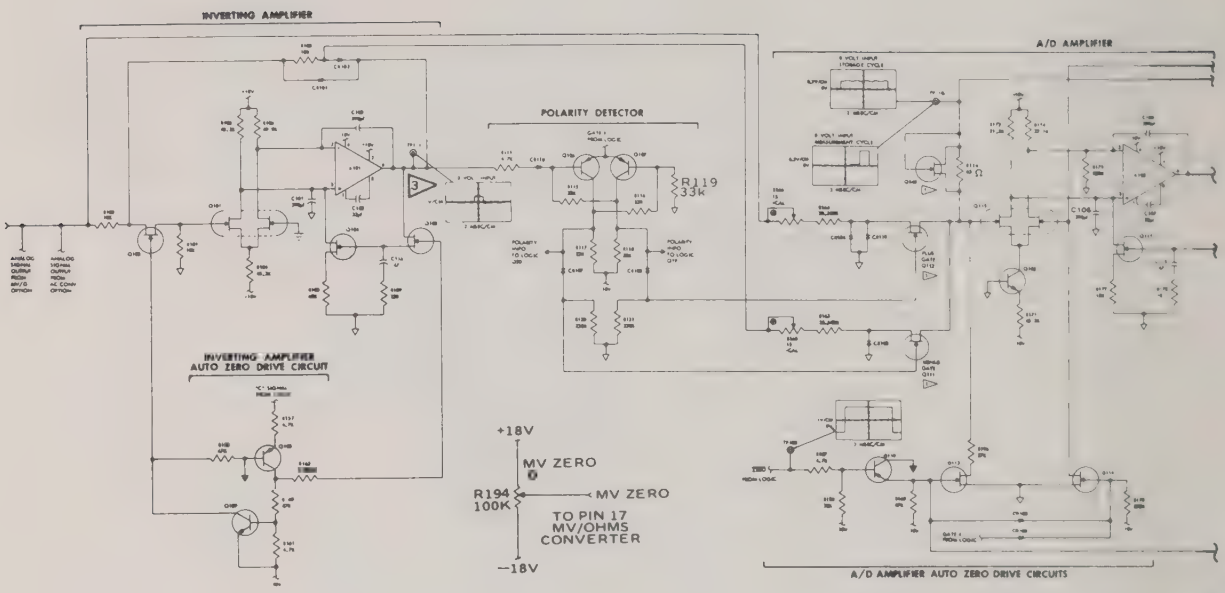


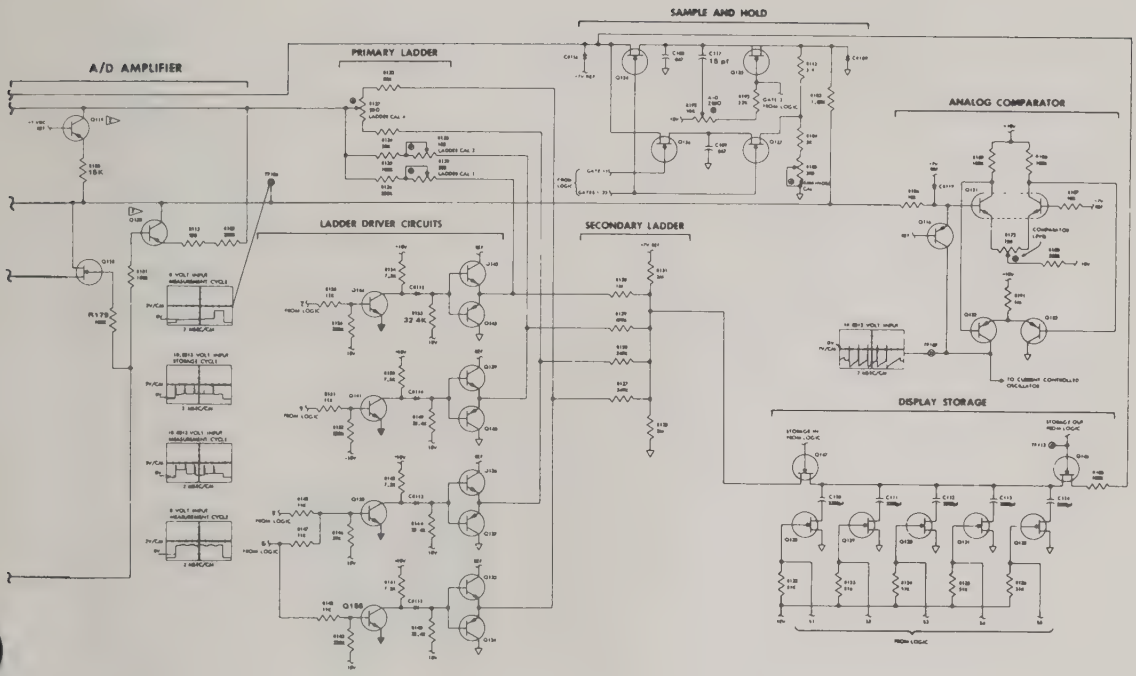
NOTES

1. ALL RESISTANCES IN OHMS AND ALL CAPACITANCES IN MICROFARADS UNLESS OTHERWISE SPECIFIED.
2. ▽ DENOTES SIGNAL GROUND
3. ▼ DENOTES LOGIC GROUND
4. *SELECTED WITH Q7
5. ⊘ DENOTES INTERNAL ADJUSTMENT

CHANGES:
(1) For S/N 123 thru 1495: R11, R43, & R44 were 1Meg-ohm. R15 & R18 were 220k.

FUNCTIONAL SCHEMATIC DIAGRAM	
MODEL 8300A BUFFER	
SCHEMATIC NO 1	
SER. NO. 123 & ON	REV. C
FLUKE JOHN FLUKE MFG. CO., INC. P.O. Box 7428 Seattle, Washington 98133	

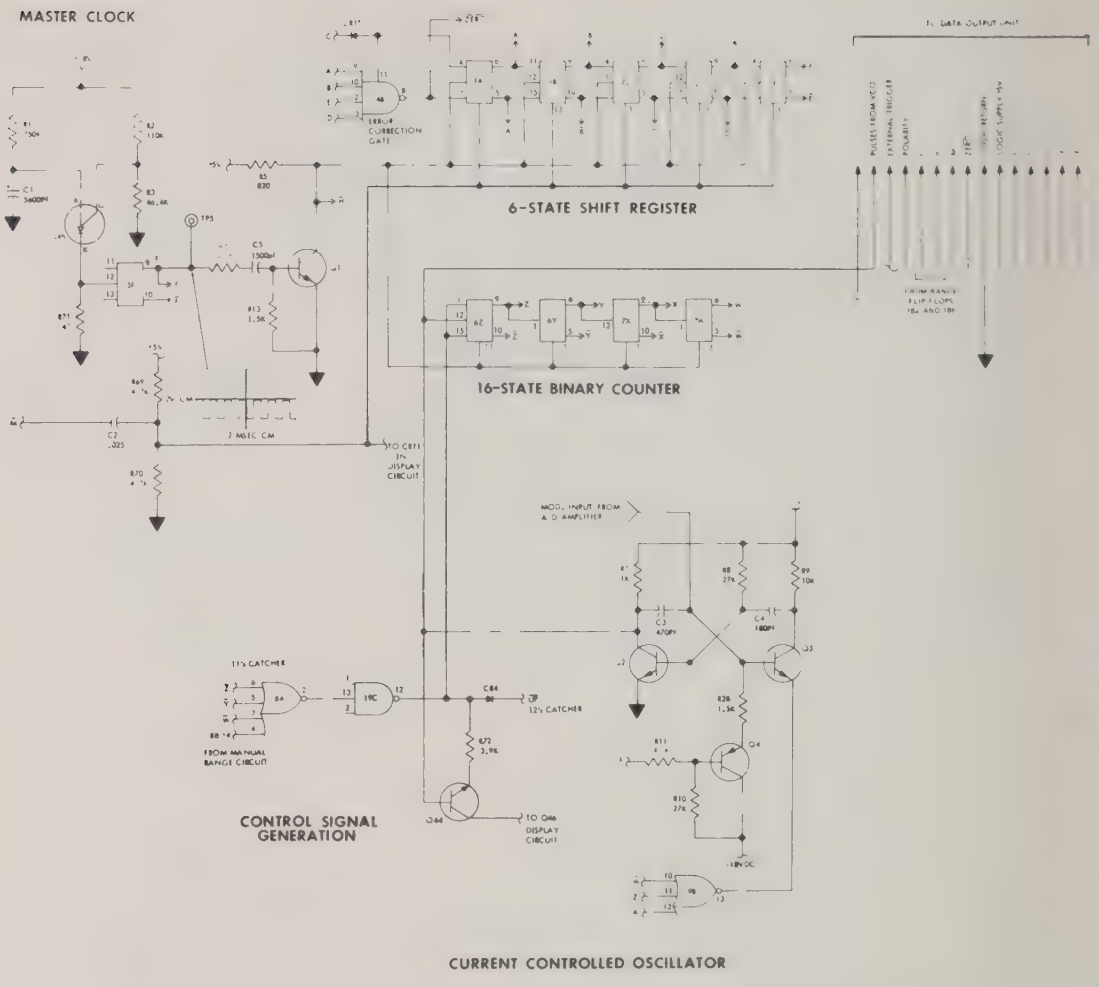

INVERTING AMPLIFIER
POLARITY DETECTOR
A/D AMPLIFIER
R119
33k
INVERTING AMPLIFIER
AUTO ZERO DRIVE CIRCUIT
+18V
MV ZERO
R194
100K
MV ZERO
TO PIN 17
MV/OHMS
CONVERTER
−18V
C106
A/D AMPLIFIER AUTO ZERO DRIVE CIRCUITS

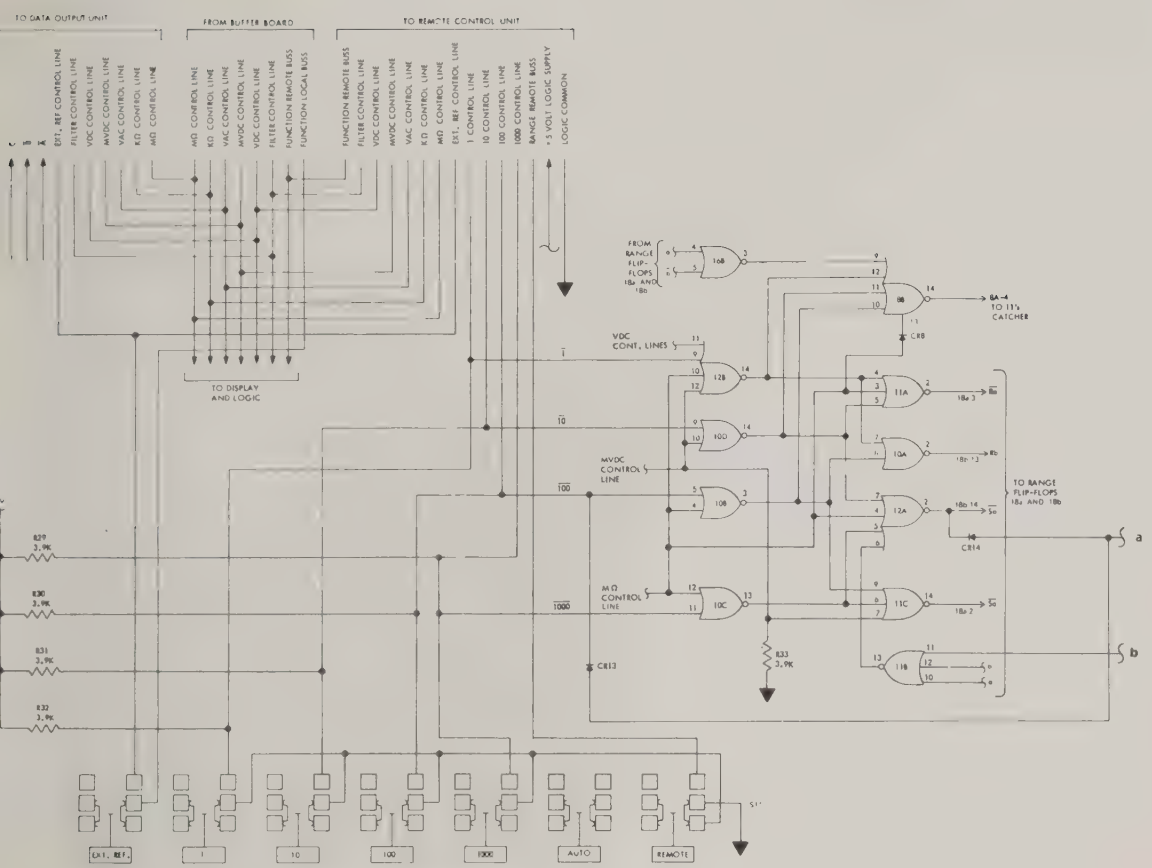


NOTES:

1. ALL RESISTANCES IN OHMS AND ALL CAPACITANCES IN MICROFARADS UNLESS OTHERWISE SPECIFIED
2. 1 DENOTES MATCHED SET
3. 2 DENOTES SELECTED TRANSISTOR
4. DENOTES SIGNAL GROUND
5. DENOTES LOGIC GROUND
6. DENOTES INTERNAL ADJUSTMENT
7. 3 STEP POLARITY MAY BE EITHER POSITIVE OR NEGATIVE, DEPENDING ON Q104 CHARACTERISTICS.

FUNCTIONAL SCHEMATIC DIAGRAM	
MODEL 8300A A/D CONVERTER	
SCHEMATIC NO 2	
SER NO 123 & ON	REV d
FLUKE JOHN FLUKE MFG. CO., INC. P O Box 7428 Seattle, Washington 98133	

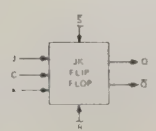

MASTER CLOCK
6-STATE SHIFT REGISTER
16-STATE BINARY COUNTER
CONTROL SIGNAL GENERATION
CURRENT CONTROLLED OSCILLATOR



FRONT PANEL PUSH BUTTONS

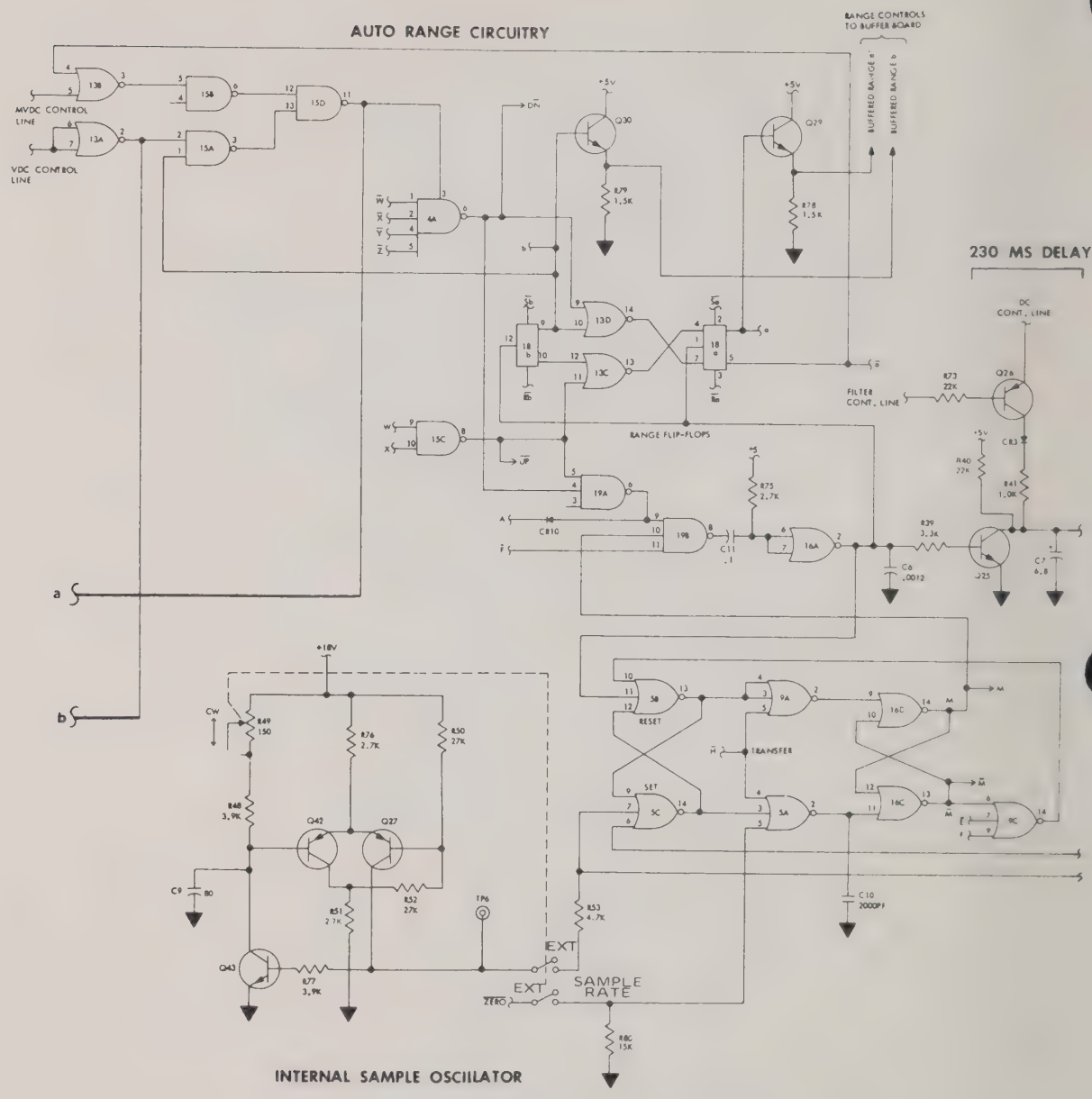
NOTES:

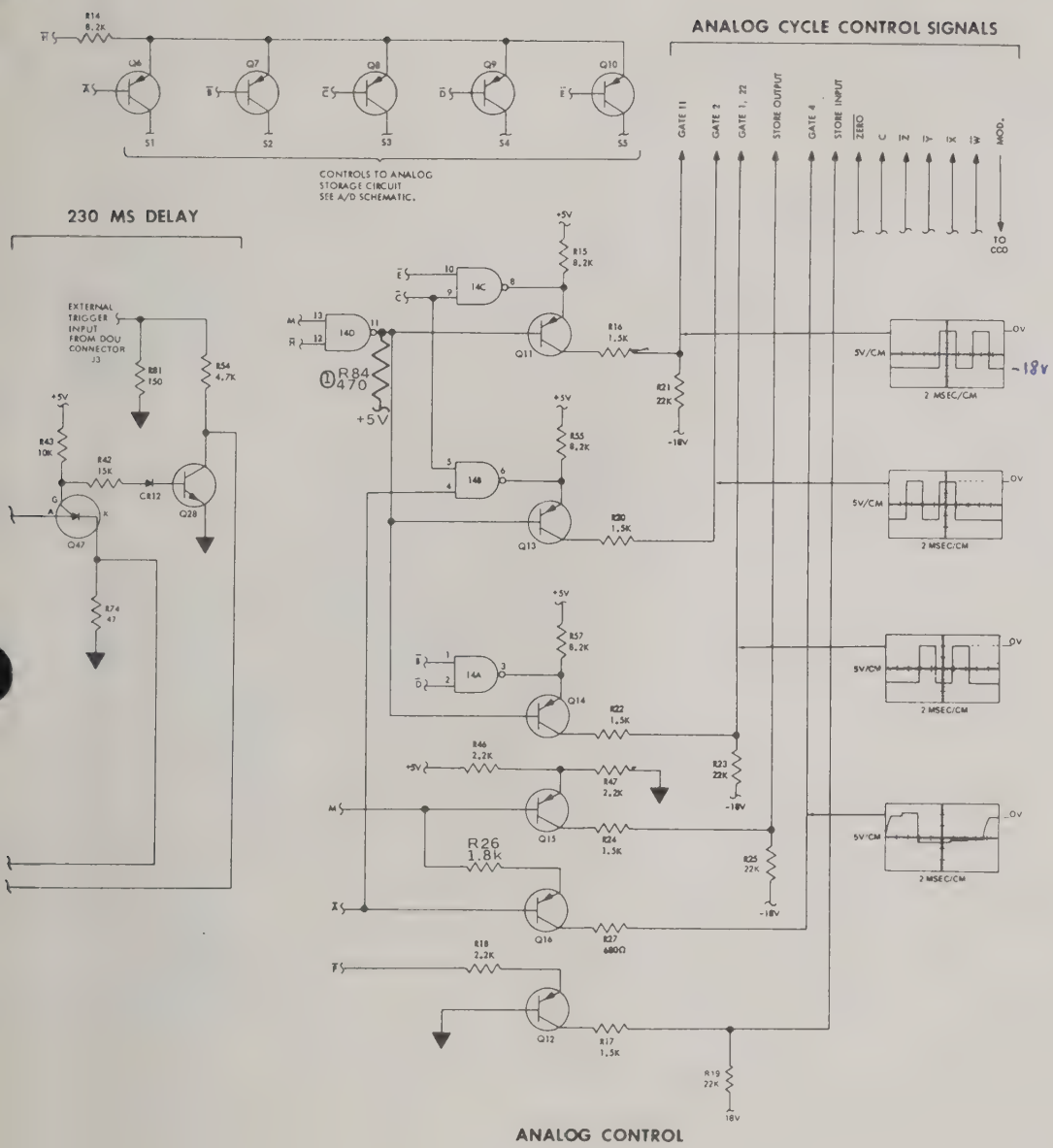
1. ALL RESISTANCES IN OHMS AND ALL CAPACITANCES IN MICROFARADS UNLESS OTHERWISE SPECIFIED.
2. FLIP FLOP KEY:



3. ▼ DENOTES LOGIC GROUND
4. * SWITCHES COMPRISING S1 SHOWN IN OFF (NON-DEPRESSED) POSITION.

FUNCTIONAL SCHEMATIC DIAGRAM	
MODEL 8300A DVM LOGIC & CONTROL SCHEMATIC NO. 3 SHEET 1	
SER NO 123 & ON	REV C
FLUKE JOHN FLUKE MFG. CO., INC. P.O. Box 7428 Seattle, Washington 98133	


AUTO RANGE CIRCUITRY
RANGE CONTROLS TO BUFFER BOARD
BUFFERED RANGE a
BUFFERED RANGE b
MVDC CONTROL LINE
VDC CONTROL LINE
230 MS DELAY
DC CONT. LINE
FILTER CONT. LINE
RANGE FLIP-FLOPS
RESET
SET
TRANSFER
INTERNAL SAMPLE OSCILLATOR
EXT
EXT
ZERO
SAMPLE RATE
a
b

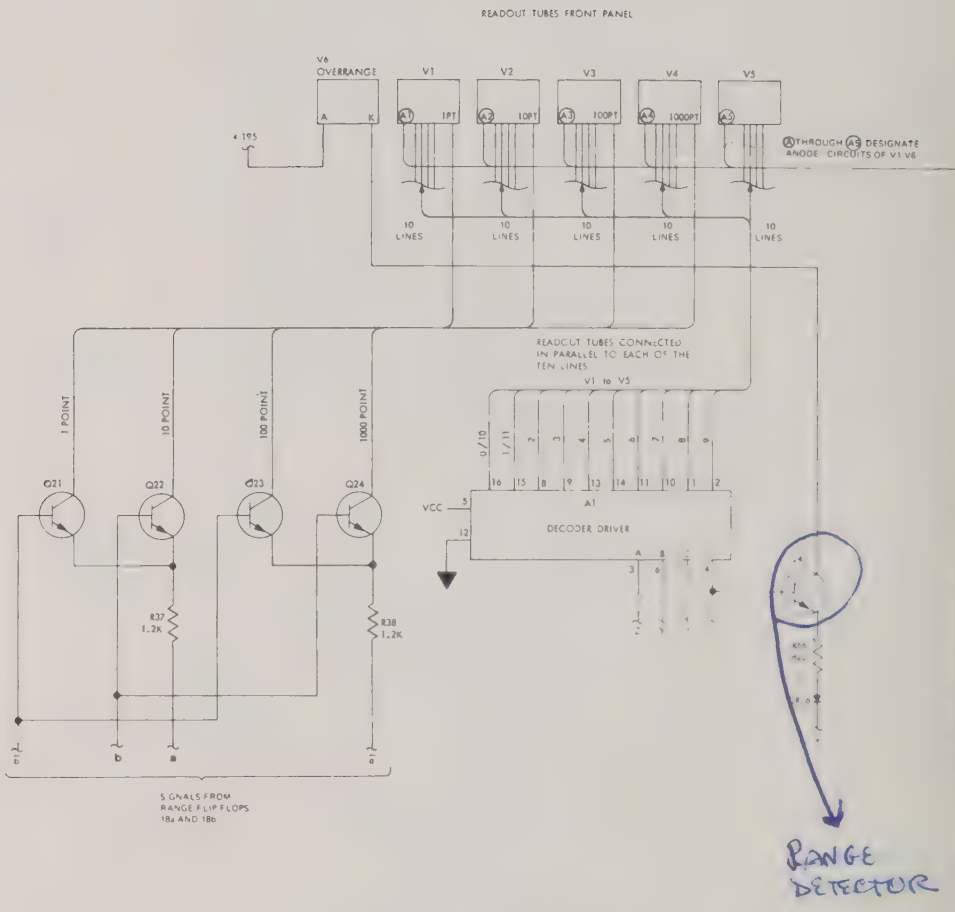


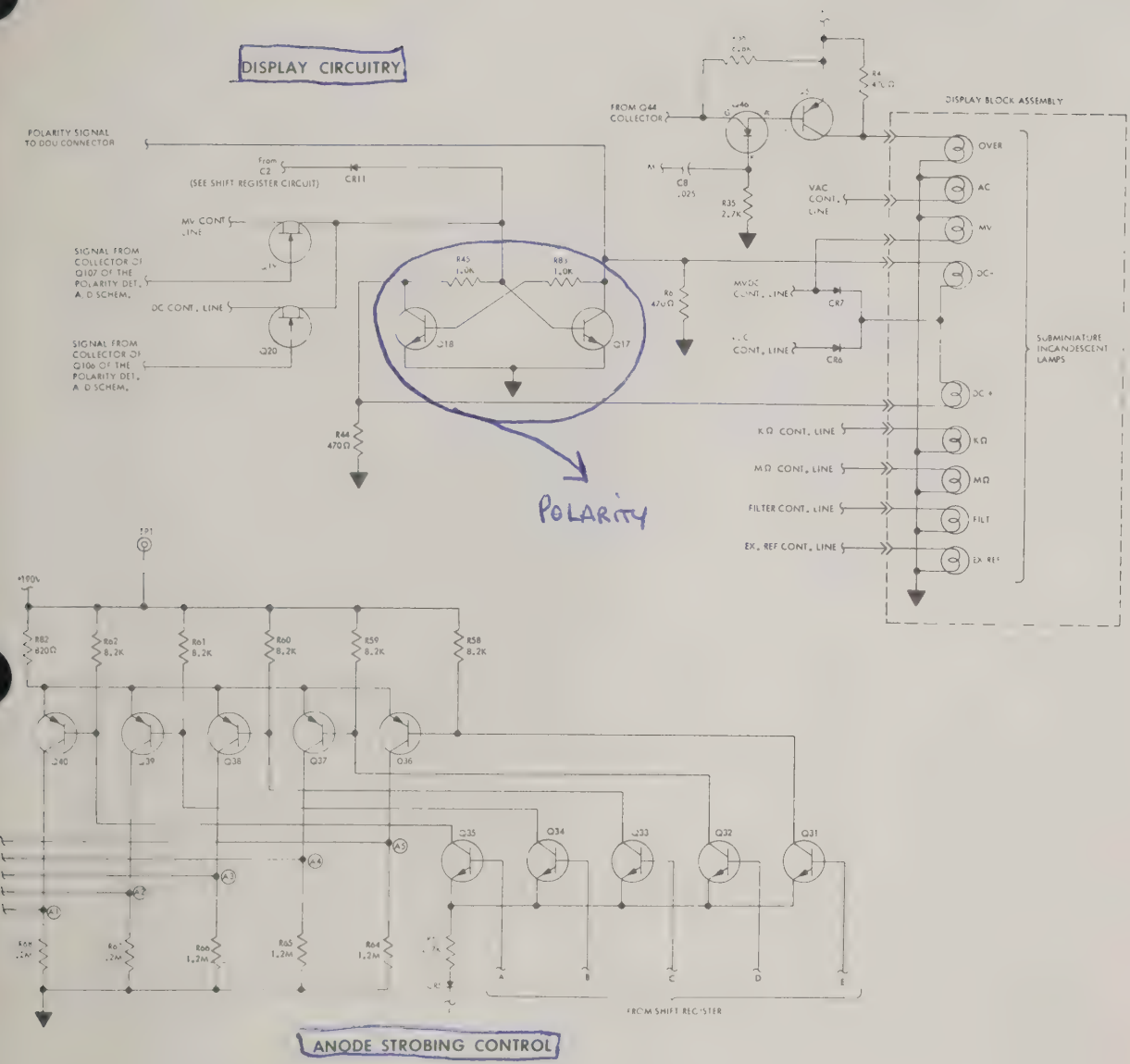
ANALOG CONTROL

CHANGES:
(1) R84 added at S/N 1750 and on.

SEE SHEET 1 FOR NOTES

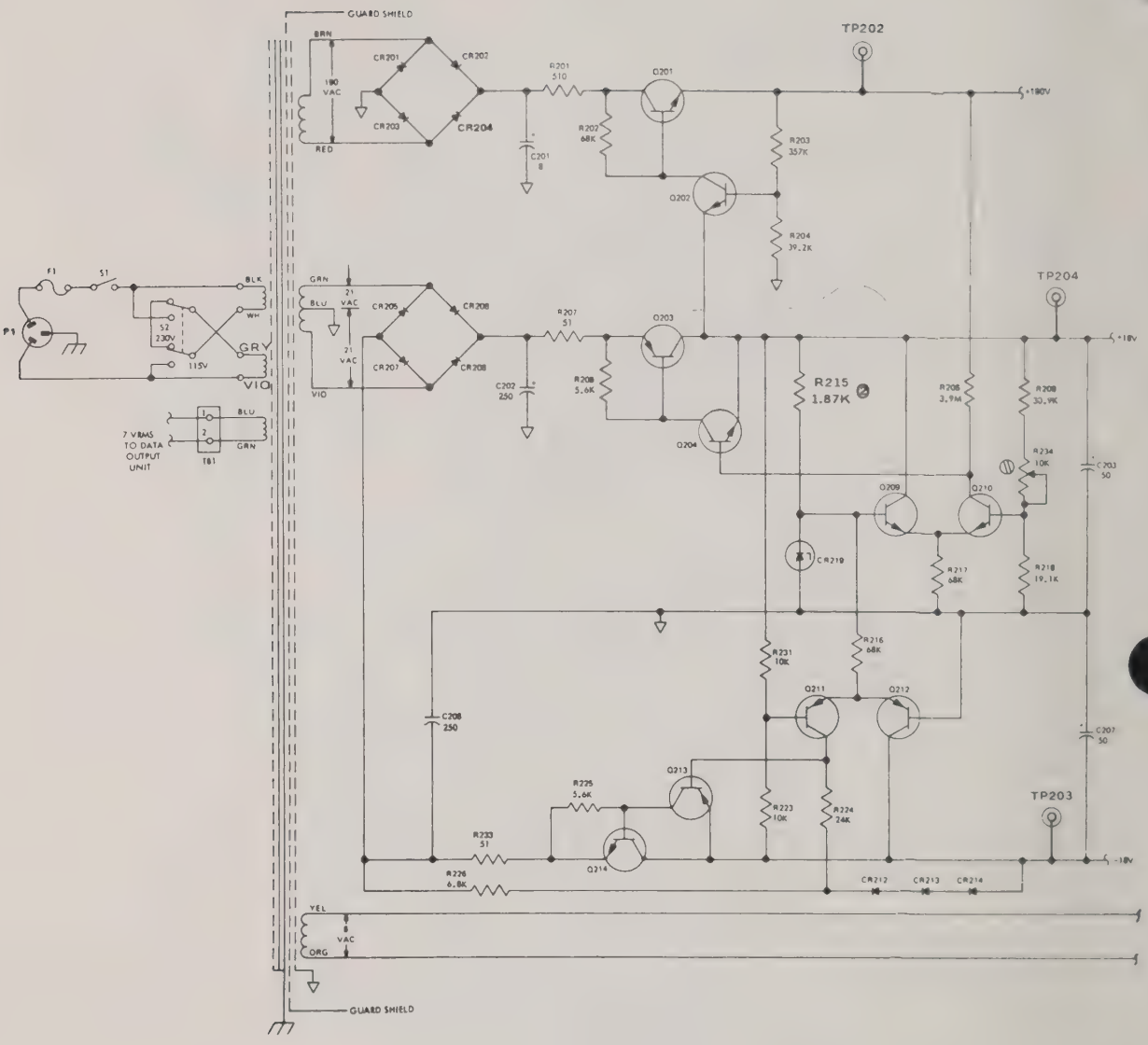
FUNCTIONAL SCHEMATIC DIAGRAM	
MODEL 8300A DVM LOGIC & CONTROL	
SCHEMATIC NO. 3 SHEET 2	
SER NO 123 & ON	REV d
FLUKE JOHN FLUKE MFG. CO., INC. P O Box 7428 Seattle Washington 98133	

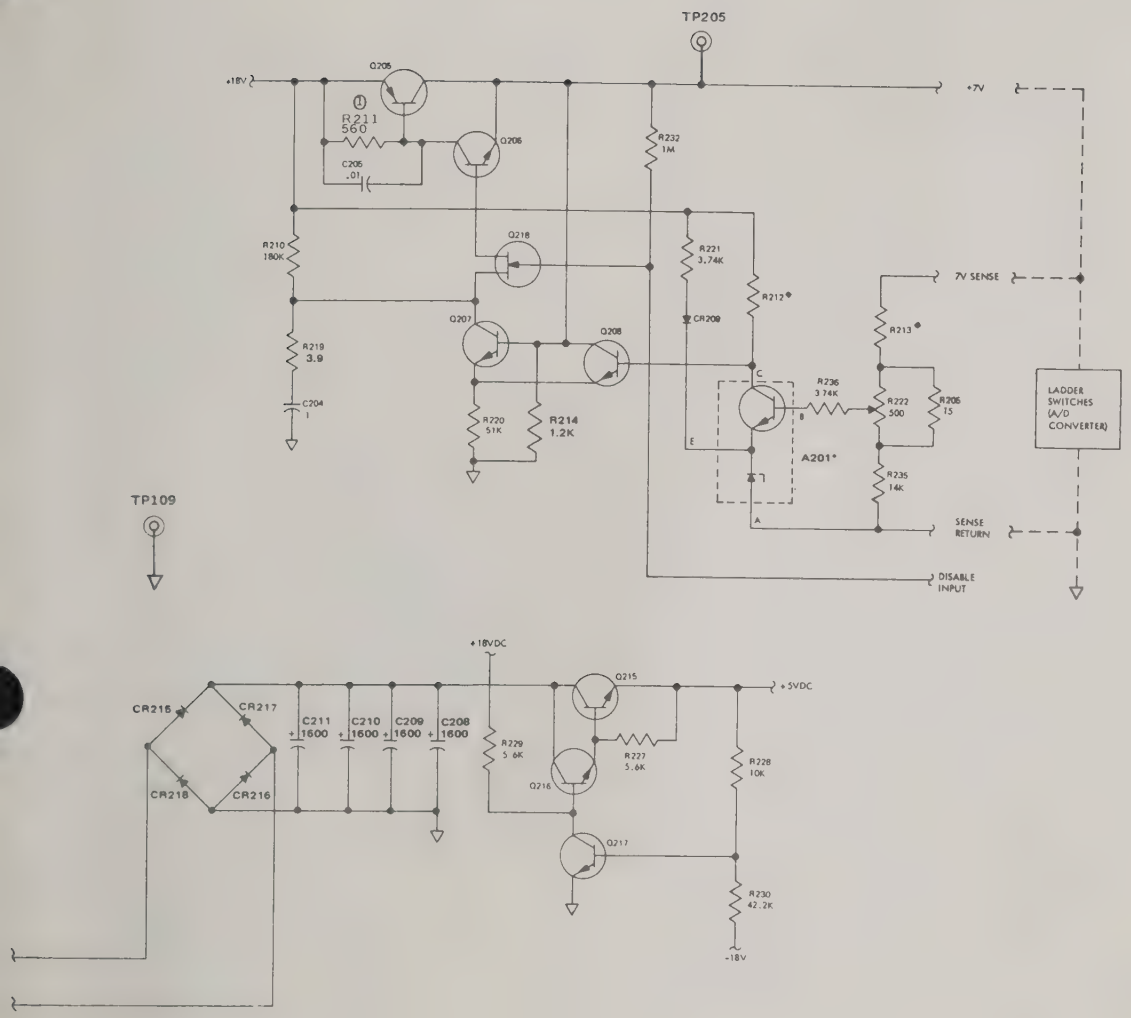

READOUT TUBES FRONT PANEL
V6
OVERRANGE
V1
V2
V3
V4
V5
A
K
A1
1PT
A2
10PT
A3
100PT
A4
1000PT
A5
+195
A THROUGH A5 DESIGNATE
ANODE CIRCUITS OF V1 V6
10
LINES
10
LINES
10
LINES
10
LINES
10
LINES
READOUT TUBES CONNECTED
IN PARALLEL TO EACH OF THE
TEN LINES
V1 to V5
1 POINT
10 POINT
100 POINT
1000 POINT
Q21
Q22
Q23
Q24
R37
1.2K
R38
1.2K
0/10
1/11
2
3
4
5
6
7
8
9
16
15
8
9
13
14
11
10
1
2
VCC
5
12
A1
DECODER DRIVER
A
B
3
6
4
SIGNALS FROM
RANGE FLIP FLOPS
18a AND 18b
RANGE
DETECTOR



NOTES:
1. ALL RESISTANCES IN OHMS AND ALL CAPACITANCES IN MICROFARADS UNLESS OTHERWISE SPECIFIED.
2. ▼ DENOTES LOGIC GROUND

FUNCTIONAL SCHEMATIC DIAGRAM	
MODEL 8300A DISPLAY SCHEMATIC NO 4	
SER NO 123 & ON	REV C
FLUKE JOHN FLUKE MFG. CO., INC. P O Box 7428 Seattle Washington 98133	


GUARD SHIELD
BRN
180 VAC
RED
CR201
CR202
CR203
CR204
R201 510
C201 8
Q201
R202 68K
Q202
R203 357K
R204 39.2K
TP202
+180V
F1
S1
P1
BLK
WH
S2 230V
115V
GRY
VIO
GRN
BLU
21 VAC
CR205
CR206
CR207
CR208
R207 51
C202 250
Q203
R208 5.6K
Q204
TP204
+18V
R215 1.87K
R208 3.9M
R208 30.9K
R234 10K
C203 50
Q209
Q210
CR219
R217 68K
R218 19.1K
7 VRMS TO DATA OUTPUT UNIT
T81
R231 10K
R216 68K
Q211
Q212
C208 250
C207 50
Q213
R225 5.6K
R223 10K
R224 24K
TP203
R233 51
Q214
R226 6.8K
-18V
CR212
CR213
CR214
YEL
8 VAC
ORG
GUARD SHIELD



NOTES:

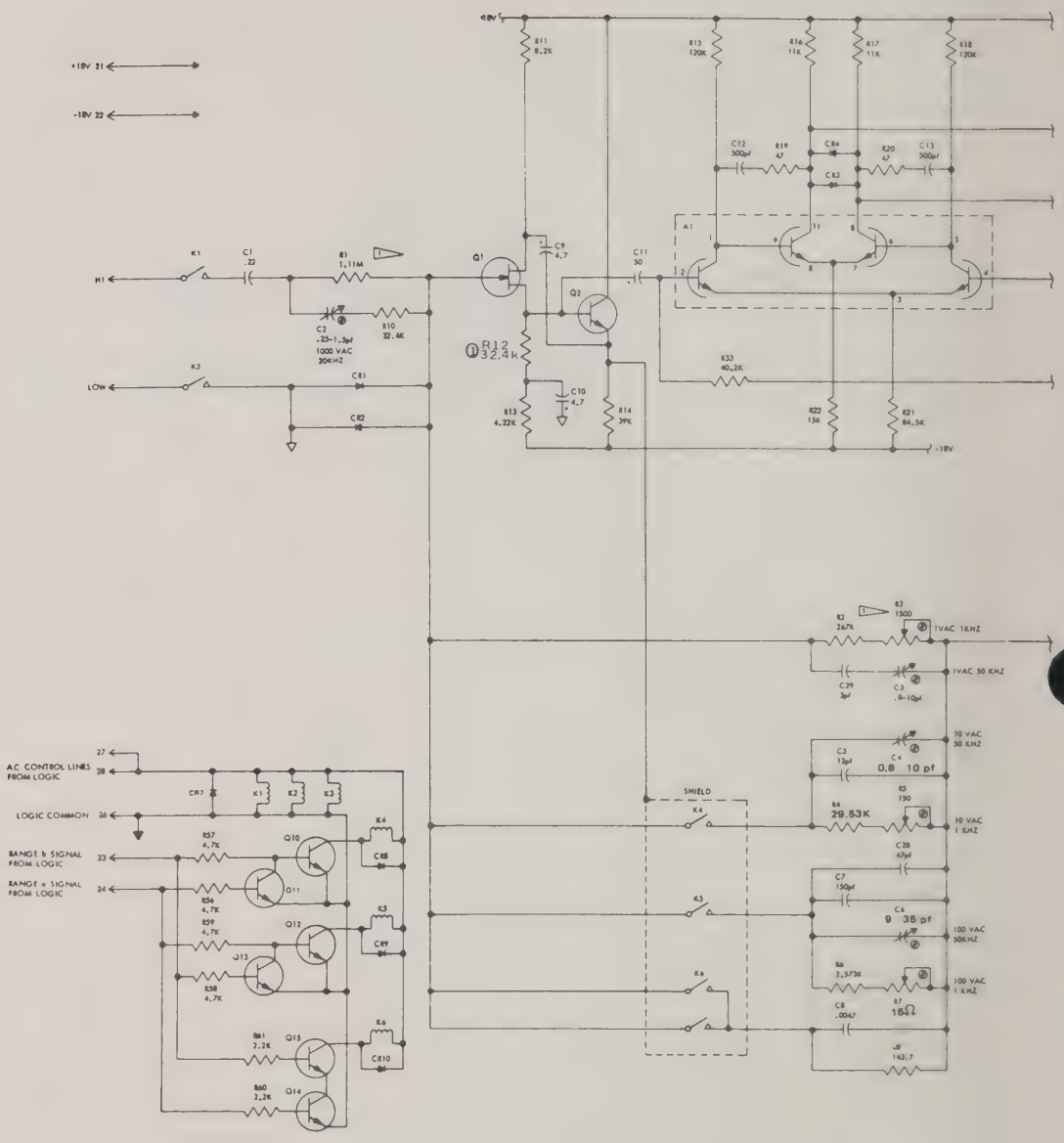
1. * DENOTES MATCHED SET
2. ALL RESISTANCES IN OHMS & CAPACITANCES IN MICROFARADS UNLESS OTHERWISE SPECIFIED
3. (1) DENOTES INTERNAL ADJUSTMENT

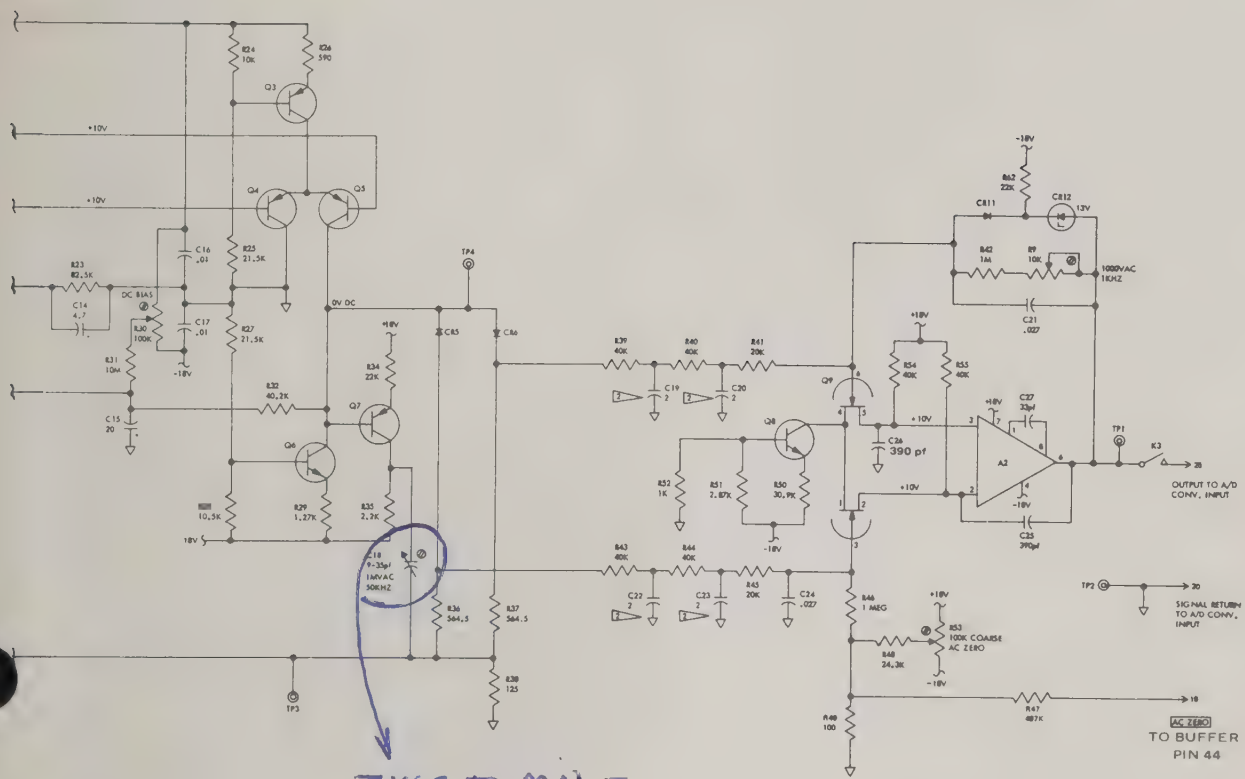
CHANGES:

(1) FOR S/N 123 THRU 1147: R211 WAS 5.6K.

(2) FOR S/N 123 THRU 1226: R215 WAS 4.22K.

FUNCTIONAL SCHEMATIC DIAGRAM	
MODEL 8300A POWER SUPPLY	
SCHEMATIC NO. 5	
SER NO. 123 & ON	REV d
FLUKE JOHN FLUKE MFG. CO., INC. P.O. Box 7428 Seattle, Washington 98133	


+18V 21
-18V 22
HI
LOW
K1
K2
C1 .22
R1 1.11M
C2 .25-1.5pf 1000 VAC 20KHZ
R10 32.4K
CR1
CR2
Q1
Q2
C9 4.7
C10 4.7
C11 50
R11 8.2K
R12 32.4K
R13 4.22K
R14 39K
R33 40.2K
R22 15K
R21 84.5K
-18V
R13 120K
R16 11K
R17 11K
R18 120K
C12 500pf
R19 47
C84
R20 47
C13 500pf
C83
A1
R3 1500
R2 267K
1VAC 1KHZ
1VAC 50 KHZ
C29 3pf
C3 .8-10pf
10 VAC 50 KHZ
C3 12pf
C4 0.8 10 pf
R5 150
R4 29.63K
10 VAC 1 KHZ
C28 47pf
C7 150pf
C6 9 35 pf
100 VAC 50KHZ
R6 2.573K
100 VAC 1 KHZ
R7 18Ω
C8 .0047
J6 142.7
SHIELD
K4
K5
K6
AC CONTROL LINES FROM LOGIC
LOGIC COMMON
RANGE b SIGNAL FROM LOGIC
RANGE a SIGNAL FROM LOGIC
27
28
26
23
24
CR7
K1
K2
K3
R57 4.7K
R56 4.7K
R59 4.7K
R58 4.7K
Q10
Q11
Q12
Q13
K4
K5
K6
CR8
CR9
CR10
R61 2.2K
R60 2.2K
Q15
Q14

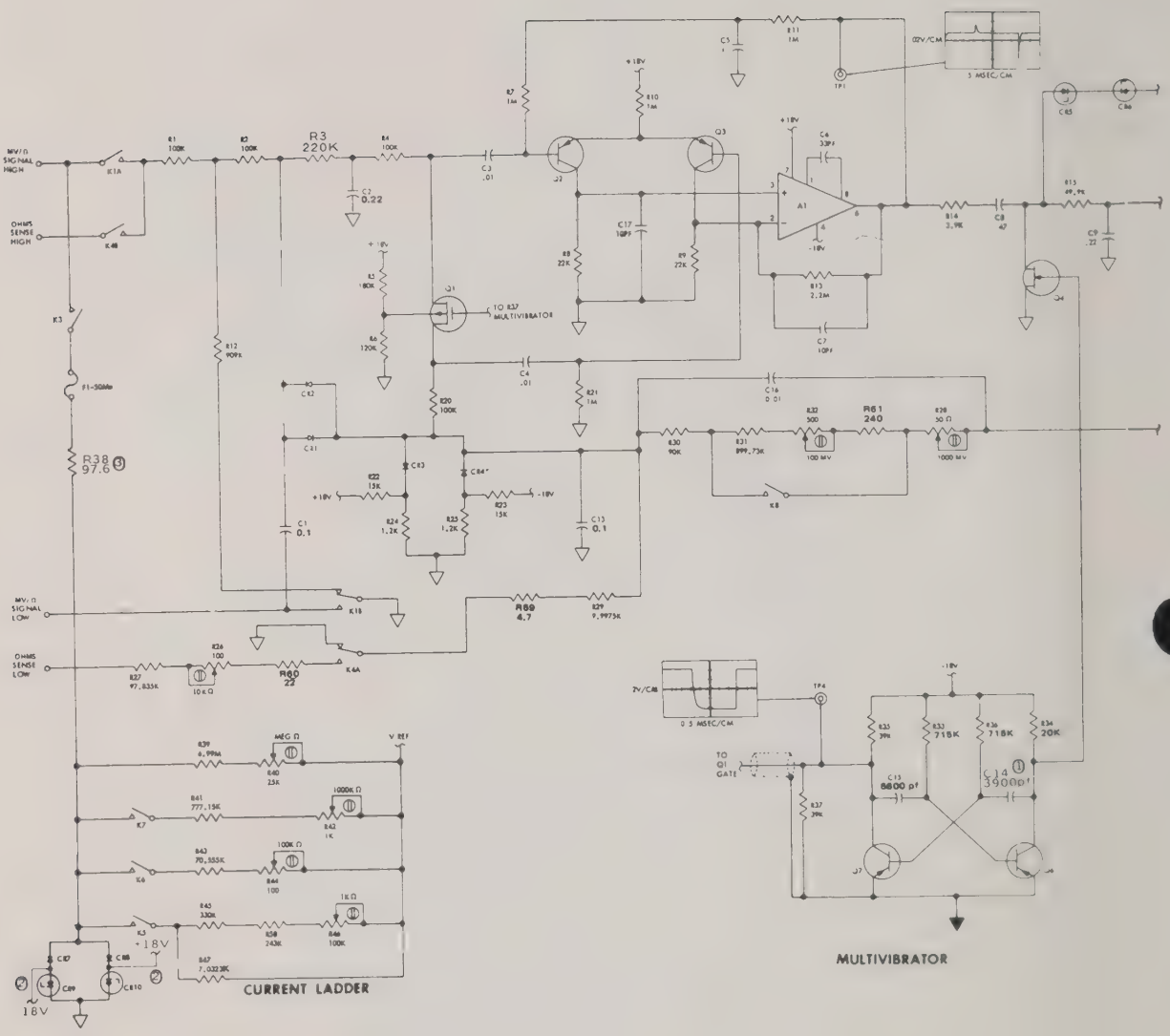


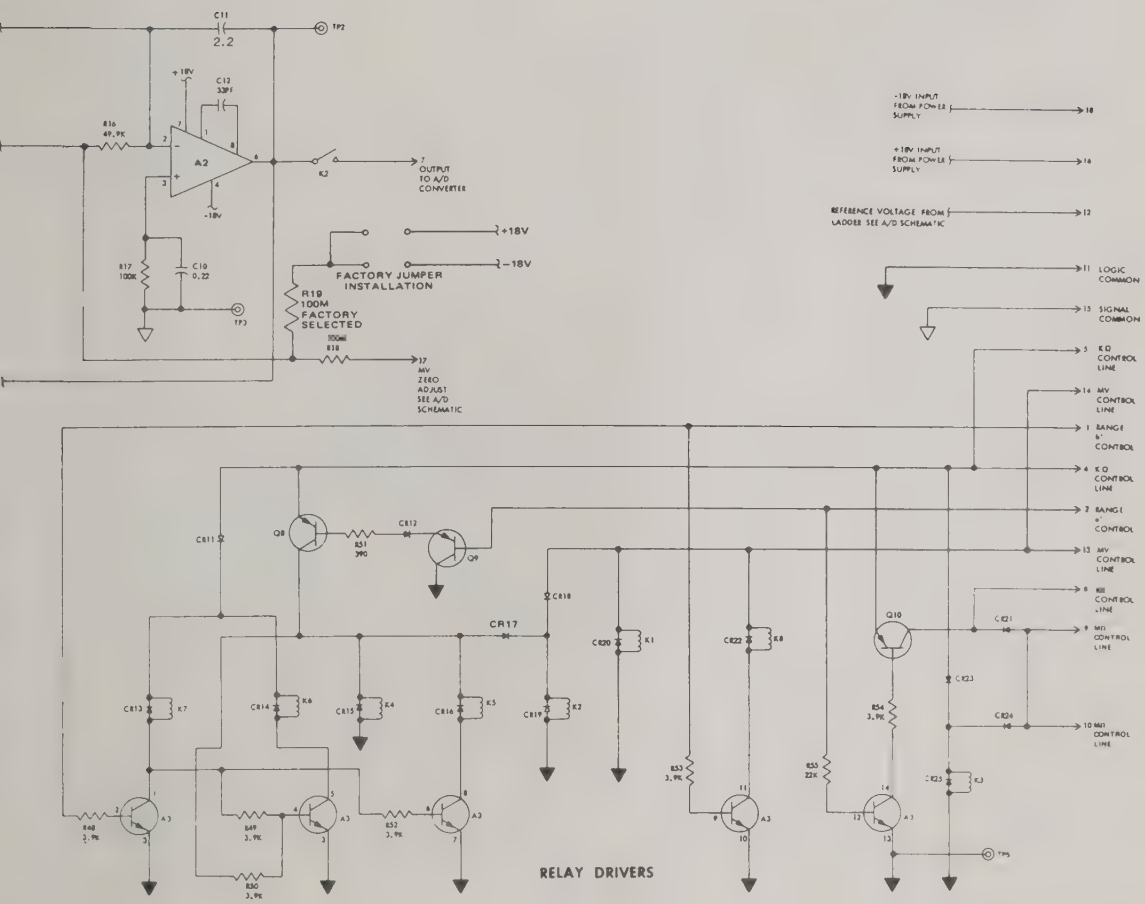
NOTES:

1. ALL RESISTANCES IN OHMS AND ALL CAPACITANCES IN MICROFARADS UNLESS OTHERWISE SPECIFIED.
2. FLAGS OF LIKE NUMBER INDICATE MATCHED COMPONENTS.
3. DENOTES FRONT PANEL CONTROL
4. DENOTES INTERNAL ADJUSTMENT
5. DENOTES SIGNAL GROUND
6. DENOTES LOGIC GROUND

CHANGES:
① For S/N 123 thru 999: R12 was 16.2k

FUNCTIONAL SCHEMATIC DIAGRAM	
MODEL 8300A AC CONVERTER	
SCHEMATIC NO. 6	
SER NO 123 & ON	REV d
FLUKE JOHN FLUKE MFG. CO., INC. P.O. Box 7428 Seattle, Washington 98133	


R3
220K
R38
97.6
R60
22
R61
240
CURRENT LADDER
MULTIVIBRATOR
TO Q1 GATE
TO R37 MULTIVIBRATOR
18V



NOTES:

1. ALL RESISTANCES IN OHMS AND ALL CAPACITANCES IN MICROFARADS UNLESS OTHERWISE SPECIFIED.
2. ▼ DENOTES LOGIC COMMON
3. ▽ DENOTES SIGNAL COMMON
4. ⊘ DENOTES INTERNAL ADJUSTMENT

CHANGES:

①For S/N 123 thru 1142:
C14 was 4700pf.

②For S/N 1438 and on:
−18V connection added to junction of CR7 & CR9.
+18V connection added to junction of CR8 & CR10.
CR9 & CR10 changed from 6.2V to 20V.

③For S/N 123 thru 1732:
R38 was 96.8Ω

FUNCTIONAL SCHEMATIC DIAGRAM

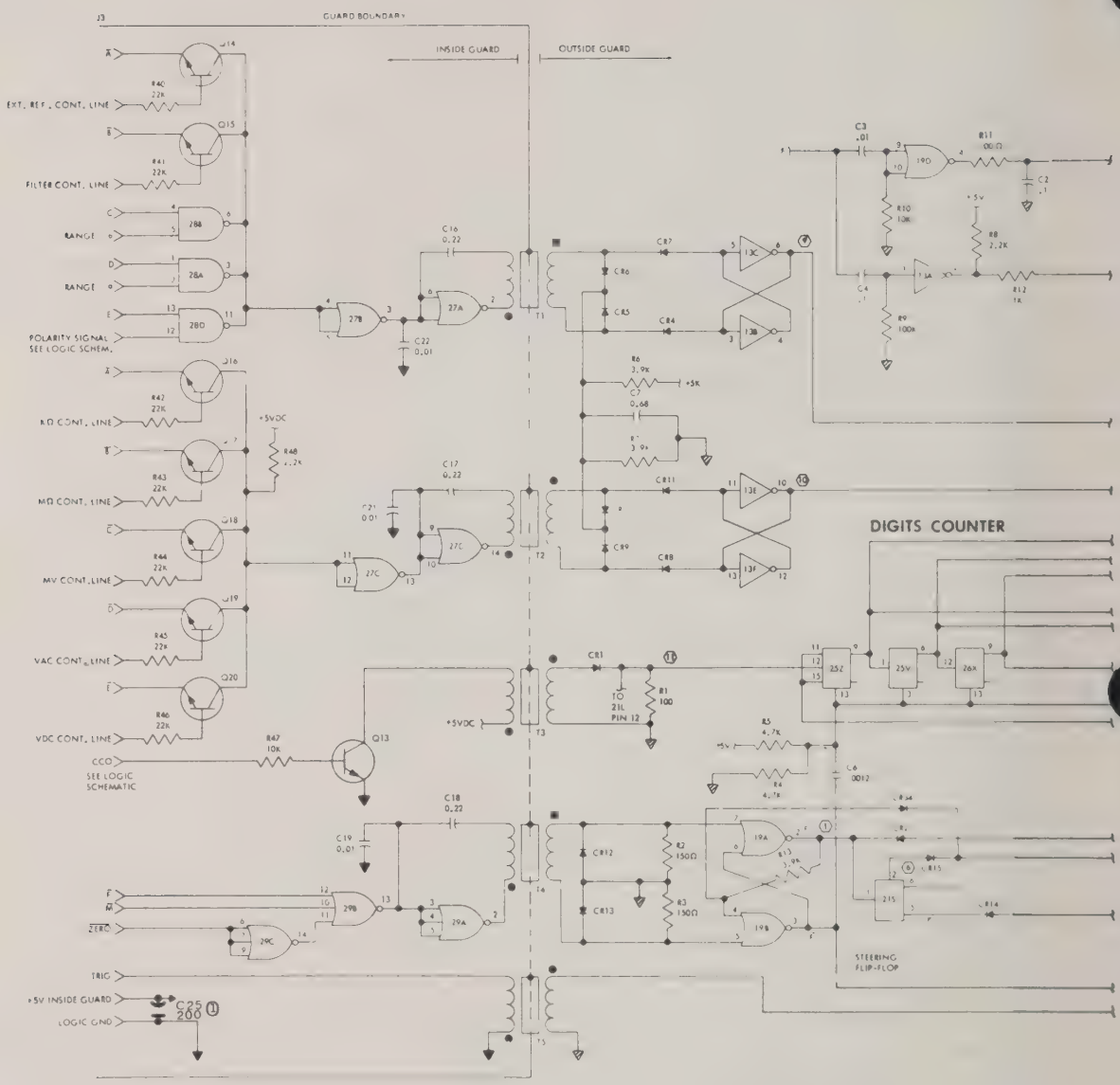
MODEL 8300A
MILLIVOLTS/OHMS CONVERTER

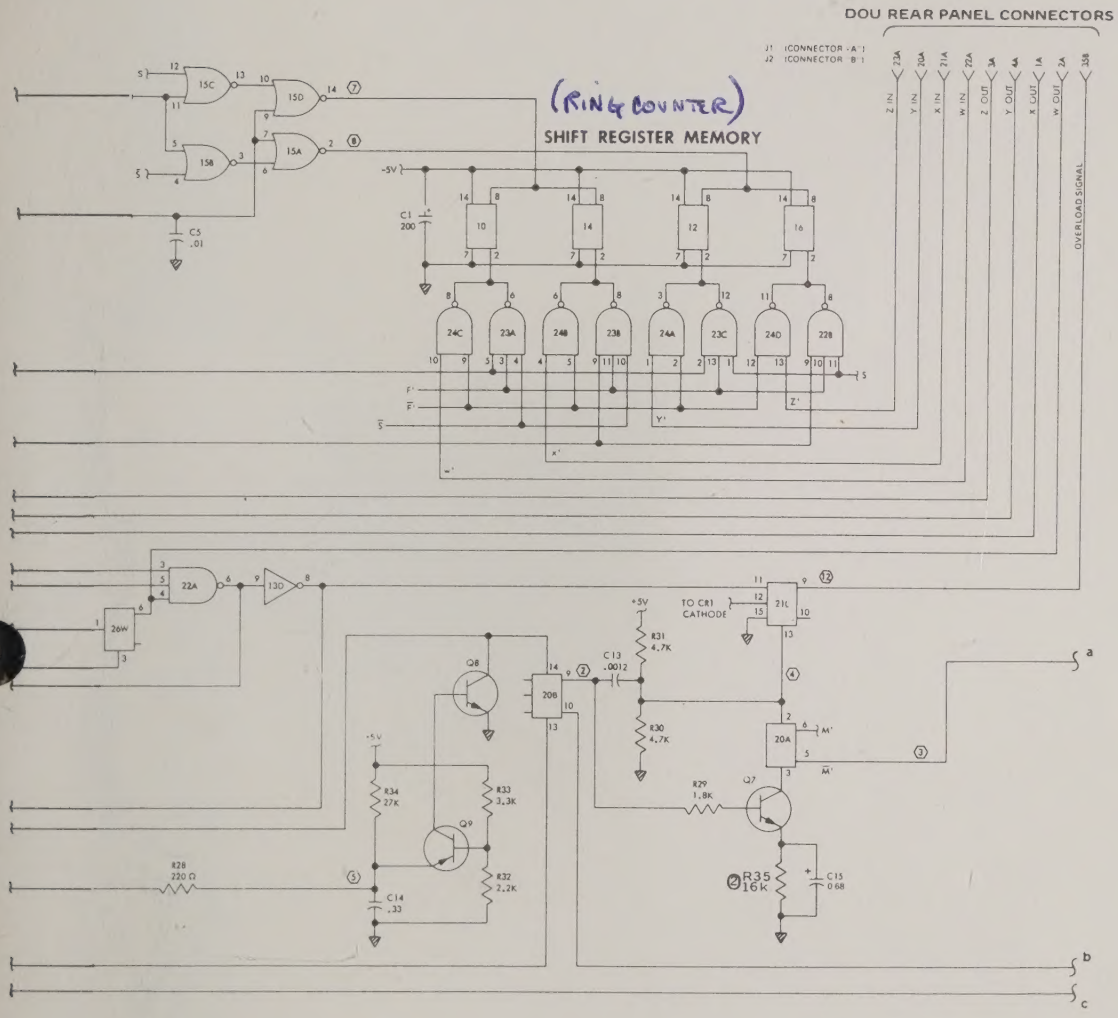
SCHEMATIC NO 7

SER NO 123 & ON

REV d

FLUKE JOHN FLUKE MFG. CO., INC.
P.O Box 7428 Seattle, Washington 98133


GUARD BOUNDARY
INSIDE GUARD
OUTSIDE GUARD
EXT. REF. CONT. LINE
FILTER CONT. LINE
RANGE
RANGE
POLARITY SIGNAL SEE LOGIC SCHEM.
MΩ CONT. LINE
MV CONT. LINE
VAC CONT. LINE
VDC CONT. LINE
CCO SEE LOGIC SCHEMATIC
ZERO
TRIG
+5V INSIDE GUARD
LOGIC GND
+5VDC
DIGITS COUNTER
STEERING FLIP-FLOP
TO 21L PIN 12



CHANGES:
1. For S/N 400 and on:
   C25, 200uf, added.
2. For S/N 123 thru 614:
   R35 was 15k.

NOTES:
1. ALL RESISTANCES IN OHMS AND ALL CAPACITANCES IN MICROFARADS UNLESS OTHERWISE NOTED.
2. ⏚ DENOTES LOGIC COMMON (INSIDE GUARD)
3. ⏚ DENOTES COMMON (OUTSIDE GUARD)
4. * DENOTES SELECTED COMPONENT
5. ROUTING OF MEMORY OUTPUTS WITHIN THE DOU IS GIVEN BY NUMERICAL DESIGNATIONS. FOR EXAMPLE, "16–P3" REFERS TO PIN 3 OF SHIFT REGISTER 16.
6. ◯ CORRESPONDS TO NUMBERED WAVEFORMS GIVEN IN FIGURES 6–4, DOU TIMING DIAGRAM.

FUNCTIONAL SCHEMATIC DIAGRAM	
MODEL 8300A DATA OUTPUT UNIT SCHEMATIC NO. 8 SHEET 1	
SER. NO. 123 & ON	REV. d
FLUKE JOHN FLUKE MFG. CO., INC. P.O. Box 7428 Seattle, Washington 98133	

NOTES: